

STATEMENT OF WORK

**University of Arkansas
Stub Number N66001-1075-8581
DARPA BAA 01-02**

CONTRACT: N66001-01-C-xxxx

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**TITLE: Algorithms and Tools for Automatic Behavioral Model Generation of
Mixed-Signal Systems-on-a-Chip**

1.0 INTRODUCTION

The objective of this project is to research and develop algorithms and tools for the generation of HDL-based behavioral models. This research will mitigate problems faced in mixed-signal System-on-a-Chip (SoC) design: design verification prior to fabrication, mixed-signal test, and synthesis of mixed-signal circuits.

Results from this research will have a significant impact on several aspects of design and test of mixed-signal SoCs. The first benefit is that behavioral models of these mixed systems will possess a greater degree of accuracy and fidelity than those available at present, while existing in a compact form for efficient execution in mixed-signal simulation. This effort lays the groundwork for further advances in modeling with respect to fault modeling and statistical behavioral modeling. This would of course impact mixed-signal test significantly. Behavioral models are the primary mechanism for representing intellectual property (IP). As more and better modeling tools become available, the ability to package IP for subsequent reuse will be greatly enhanced. This, in turn, strongly influences mixed-signal SoC cycle times because ICs of this complexity depend heavily upon reuse. Lastly, the higher fidelity behavioral models that result from this research enable accurate simulation-based analog and mixed-signal synthesis.

2.0 BACKGROUND

The design of mixed-technology systems is a key driver for several DoD applications. These include a variety of systems such as communications, information, and biological systems. In most applications that are deployed in the field, portability and low power are important considerations.

Remote sensing combined with communication is an essential component of the following DoD systems: biological warfare defense, surveillance and targeting, sensor and navigation, and combat. For any of these applications complex integrated systems

have to be designed that include a collection of diverse technologies (e.g., electronics, photonics, mechanical, fluidics, biological, and chemical). These highly complex nonlinear mixed-technology systems have to be designed and verified before prototyping. Simulation and modeling play a significant role in predicting the performance of systems before an actual implementation.

Given the level of complexity of these systems, it is essential that a top-down design methodology be used during design rather than the conventional approach of a bottom-up design methodology. The latter is not very cost effective and does not easily allow for system level modifications. However, a top-down design methodology requires both a systematic modeling approach and a framework that facilitates the task of defining, designing, and validating a system, sub-system, and the underlying components. This will mitigate problems associated with designing complex integrated systems and yield systems that are correct by construction. The basis for a top-down design methodology is accurate and fast behavioral models and a framework that supports a top-down design approach.

Although there has been considerable work done in the design automation of integrated circuits, a systematic and consistent approach for top-down design does not exist even for integrated RF, analog and digital systems. No tools exist that allow all three technologies to be simulated effectively in one simulator. The development of mixed-signal hardware description languages has enabled more effective simulation of analog and digital. However, those simulators are just now becoming commercially available. So, while the simulation technology has begun to arrive, design bottlenecks still exist for integrated circuits. Behavioral models represent a means to easing this bottleneck.

Tools for behavioral model generation will eventually enable analog/RF synthesis, architectural exploration and design for test. The ability to rapidly evaluate the quality of a design candidate is the core of synthesis. Unlike digital synthesis, the evaluation of a candidate analog/RF design, even if it is small in size, requires expensive simulation time. With simple yet accurate behavioral models, design candidate evaluation can be done quickly so that design exploration and synthesis can be realistic. Similarly, the ability to rapidly access the faulty effect caused by manufacturing defects is vital to the adoption of the design for test methodology.

3.0 SCOPE

This proposal consists of interrelated investigation and development efforts. Each of these areas has technology development needs that are pivotal for effective top-down design and design verification of mixed-signal SoCs. These efforts are outlined below:

1. Bottom-up behavioral model generation and model order reduction

- Dominant pole-zero identification based equation extraction from circuit netlists
- Determinant-decision-diagram based symbolic analysis for behavioral model generation

2. Behavioral modeling tools prototype

- Modeling tool prototype for HDL code generation
- Modeling tool prototype for model validation and characterization
- Modeling tool prototype for capturing atypical behaviors (noise, thermal)
- Modeling tool prototype for model creation and model order reduction

4.0 TECHNICAL REQUIREMENTS

4.1 Basic Task Details

4.1.1 Bottom-up behavioral model generation and model order reduction

There are two thrust areas of this investigation. However, each of them has as a primary objective: the development of systematic methods for automatic generation of compact behavioral models from circuit netlists. The class of circuits targeted in this investigation include building blocks in wireless communications and base band analog processing such as operational amplifiers, LNAs, power amplifiers, mixers, and phase-locked loops. Some of the primary behavioral characteristics to be generated include various circuit transfer functions such as DC and AC gains, input and output impedance. Further, nonlinear dynamics will be a major focus of these investigations. While these two thrusts have significant overlap in goals, the approaches are quite different. The collaboration should lead to an excellent tool for bottom-up behavioral modeling.

In addition, research will be directed toward incorporating the proposed techniques and CAD tools into a general behavioral modeling environment.

4.1.1.1 Dominant pole-zero identification based equation extraction from circuit netlists

This method is hereafter referred to as the *DAE method* after the fact that differential algebraic equations (DAEs) are extracted from the original circuit. Primary research subtasks shall include:

- **Identify specific circuits in a mixed-signal SoC testbed to which the DAE approach will be applied.** Working with one of the testbed SoC designers, various blocks in the design will be chosen for focus – expanding to the remainder later in the project. This testbed, a mixed signal SoC design serving as an interface with a MEMS microgyroscope chip and managed by Jet Propulsion

Laboratory (JPL), shall be a focal point for behavioral modeling research and a vehicle for validating results.

- **Enhance and implement the DAE modeling research.** The previous research consists of a collection of programs to perform analysis. This task shall involve enhancing this previous work by utilizing more up-to-date algorithms for linear analysis, automating table extraction and equation formulation, and improving the signal path-tracing algorithm for analog and RF circuits.
- **Extend the application of the *DAE method*.** Based on the circuits in the testbed and others identified by DARPA, extend the method to a broader class of circuits.

4.1.1.2 Determinant-decision-diagram based symbolic analysis for behavioral model generation

The work will be based on an innovative concept called determinant decision diagrams (DDD) that enables precise yet compact representation of exact circuit symbolic expressions. The major focus of this research shall be directed to nonlinearity modeling, noise modeling and pole/zero characterization. Primary research tasks include:

- **DDD complexity and minimization.** Exact and heuristic algorithms for ordering DDD vertices shall be developed and implemented, so that the resulting DDD is minimal. A minimal DDD representation will save memory space required to store symbolic expressions, and enable more efficient manipulation of symbolic expressions for behavioral model generation.
- **Mixed symbolic and numeric analysis.** Techniques shall be developed to generate behavioral models for circuits where part of the parameters are symbols and the rest are numerical numbers. By combining symbolic and numeric analyses, compact yet parametric models shall be obtained.
- **Efficient symbolic pole/zero generation.** Poles and zeros of transfer functions provide the stability information. Algorithms to generate symbolic pole and zero expressions shall be developed, so that insight can be gained on which parameters affect circuit stability.
- **Distortion analysis.** Symbolic analysis research effort shall be directed to distortion analysis for communication circuits. Volterra series methods will be explored with the DDD concepts.
- **DDD-based approximation of symbolic expressions.** Algorithms that can generate approximate symbolic expressions for a given accuracy requirements will be explored as well.

4.1.1.3 Merger of DDD and DAE methods

The *DAE method* shall be merged with the DDD-based technique, utilizing symbolic analysis in place of pure numerical analysis for some key steps. This highly collaborative effort shall seek to marry the best features of each modeling approach. Inclusion of symbolic methods into the DAE method and inclusion of root localization methods into the DDD pole-zero extraction shall be investigated.

4.1.1.4 Research validation

Models generated from this research will be validated against circuit level simulations of the originating designs. This effort is reduced in scale from full SoC testbed validation. Data available from the NeoCAD program may be used as part of this validation.

4.1.2 Behavioral modeling tools prototype

The focus of this task is a working prototype of behavioral modeling tools for technology. The behavioral modeling environment, including top-down design flows, verification needs, and formulation of the system requirements, shall be established. The environment and software architecture shall be designed.

4.2 Program Management and Reviews

4.2.1 Program Management Plan

The Contractor shall develop a Program Management Plan. A graphical representation of this plan (a Gantt Chart is one example) identifying major tasks and their leaders, milestones of the major tasks and their completion dates shall be generated. In addition the Program Management Plan shall address technology transition of the products of Section 5.2.

4.2.2 Transition Plan

The Contractor shall develop and maintain an updated Transition Plan. Due to the scope of the project involving primarily basic behavioral modeling algorithm research (and the validation of that research), the transition plans shall consist mostly of publishing technical articles at conferences and in peer-reviewed journals. In addition, technical reports shall be generated.

4.2.3 Kick-off Meeting

The Contractor shall participate in a kick-off meeting within 100 days of contract award. The purpose of this meeting is to introduce key program personnel, discuss the proposed tasking, present the program schedule and milestones, and present the initial Program Management Plan.

4.2.4 Reviews

The Contractor shall hold quarterly reviews for the duration of this effort. Two of the quarterly reviews can be held at the Contractor's site. The purpose of these reviews is to present a summary of work completed and milestones met, discuss any problems encountered, update the program schedule, present the program financial status, and discuss remaining work.

Annually, one of these reviews shall be an open review held for all of the Principal Investigators of the NeoCAD program to present the status of their work. A closed review section to discuss program details for the Contractor may also be held concurrently.

4.2.5 Final Contract Review

The Contractor shall host a final contract review held in place of the last quarterly review. The purpose of this review is to present a summary of all work completed and milestones accomplished and to discuss any relevant future efforts similar to the contract, which may be pursued.

4.2.6 Publications

The Contractor shall provide SPAWARSYSCEN a copy of publications at the time they are submitted for publication.

4.2.7 Travel

Travel will be required for contract review purposes for two of the four quarterly reviews. The Contractor should plan on each trip lasting three days. One review will be an open review held for all of the Principal Investigators of the NeoCad program. The location of this meeting will vary. One of the quarterly review meetings may be held at SPAWAR Systems Center - San Diego.

In addition, the Contractor should plan on attending a yearly ‘Topical Meeting of Principal Investigators’. The location of this topic-driven meeting will most likely take place in Washington, D.C.

5.0 DELIVERABLES

5.1 Reporting

The reports and presentation materials are to be delivered in accordance with the attached CDRLs.

5.2 Products

This project will provide the following capabilities:

Bottom-up behavioral model generation and model order reduction

- Dominant pole-zero identification based equation extraction from circuit netlists
- Determinant-decision-diagram based symbolic analysis for behavioral model generation

Behavioral modeling tools prototype design, which will include

- Modeling tool prototype for HDL code generation
- Modeling tool prototype for model validation and characterization
- Modeling tool prototype for capturing atypical behaviors (noise, thermal)
- Modeling tool prototype for model creation and model order reduction

5.3 Milestones

The goal for realization of the identified milestones are as listed.

MILESTONE	Year 1	Year 2	Year 3
1.0 Bottom-up behavioral model generation and model order reduction			X
1.1 Dominant pole-zero identification based equation extraction from circuit netlists			X
1.1.1 Identify specific circuits in testbed to which the DAE approach will be applied	X		
1.1.2 Enhance and implement the DAE modeling research	X		
1.1.3 Extend the application of the <i>DAE method</i>		X	
1.2 Determinant-decision diagram based symbolic			X

analysis for behavioral model generation			
1.2.1 DDD complexity and minimization	X		
1.2.2 Mixed symbolic and numeric analysis		X	
1.2.3 DDD-based approximation of symbolic expressions.		X	
1.2.4 Efficient symbolic pole/zero generation.	X		
1.2.5 Distortion analysis			X
1.3 Merger of DAE and DDD methods			X
1.3.1 Inclusion of symbolic methods into <i>DAE method</i>			X
1.3.2 Inclusion of root localization method into DDD pole-zero extraction			X
1.4 Research validation			X
1.4.1 Measurements of testbed circuits		X	
1.4.2 Development of validation suites		X	
1.4.3 Model validation			X
2.0 Behavioral modeling tools prototype design			X

6.0 SECURITY CLASSIFICATION

This effort is unclassified.

7.0 OTHER

7.1 Government Points of Contact

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