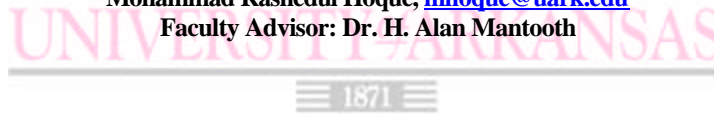


# SWITCHED CAPACITOR STEP UP DC/DC CONVERTER FOR SYSTEM-ON-A-CHIP

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**ABSTRACT** – Several DC/DC converters have been designed, laid out and tested to improve the pumping efficiency, ripple voltage and to get high output voltage. Switch-capacitor based design has been implemented and the use of inductor was vetoed to reduce the size, non-linearity and interference. Silicon-On-Insulator (SOI) technology has been implemented to overcome the limitation of getting high output voltage (60 volts) of a system-on-a-chip. In several cases MOSFET body diode is used as a charge transfer switches (CTS) to reduce the cut-in voltage and consequently to improve the overall pumping efficiency. The body diode is characterized and a SOI NMOS body diode model is developed for simulating the charge pump circuit. A novel DC/DC converter has been designed and laid out to get better pumping efficiency and low output ripple voltage.

**BACKGROUND** - As electronic devices decrease in size and increase in computing power, integrated circuit components must decrease proportionally as well, resulting in the need for low-power, low-voltage techniques in both digital and analog systems. This is especially true in battery-powered electronic equipment where only one source of power is available and various voltage levels are desired.

Two popular topologies for stepping DC voltages are the charge pump DC/DC converter (CPC) and the boost switching DC/DC converter (BSC). BSC can provide much more power than CPC, and its efficiencies are more than 90%, but the BSC requires large inductors.

There are several disadvantages of using inductors. If the inductor is big, it will occupy a large space on the chip. It also generates magnetic fields, which may cause problems for the other circuits of a System-On-a-Chip (SOC). The use of inductors should be avoided because of their size, non-linearity and interference.

The most compelling advantage of a CPC is the absence of inductors. It is well known that it is very difficult to integrate inductors on a chip. Obviously, when size becomes an issue and the load is very light, CPCs offer characteristic advantages over BSCs. CPCs are designed using capacitors and switches such as MOSFETs or diodes. Since charge pumps do not require inductors, they can be implemented entirely on-chip.

**WORK DONE** - Several different types of CPC have been studied and investigated. Among them several improvements have been made on Dickson and Favrat charge pump converters to get the expected results. A new charge pump converter has been designed to get better performance.

The voltage pumping gain for a Dickson charge pump implemented in a partially depleted (PD) 0.35  $\mu\text{m}$  radiation-hardened silicon-on-insulator (SOI) CMOS process is increased when compared with a traditional bulk CMOS Dickson charge pump. The threshold voltage drop due to the body effect of the diode-connected MOSFET CTS is suppressed using the body diode of a NMOS transistor in SOI technology. A 6-stage Dickson charge pump is designed to produce a 20 V output from a 3.3 V supply, with a 4 MHz, two-phase non-overlapping clock signal driving the charge pump. An efficiency of 72% is achieved at a load current of 20  $\mu\text{A}$ .

Designed and laid out a 18-stage Favrat charge pump circuit, which will produce 60 V at the output from a 3.3V supply. Several improvements have been made on conventional Favrat charge pump. SOI PMOS has back-gate effect for high switching voltage. Therefore, to achieve high output voltage NMOS body-diode has been implemented instead of PMOS switches. The circuit was laid-out for Honeywell Partially Depleted 0.35  $\mu\text{m}$  MOI5 3.3 V SOI rad-hard process.

Designed, simulated, and laid out a novel DC/DC converter to produce 15 V from a 5 V supply. The circuit is designed by combining Dickson and Favrat topologies. The circuit has 99% pumping efficiency and power efficiency is around 70%. It is designed for Tower Semiconductor 5 V, 0.5  $\mu\text{m}$  bulk process.

**FUTURE WORK** - Fabrication of 60 volts charge pump is already done by Honeywell. The die will be packaged and send to us sometime during spring 2003. The biggest challenge is to test the chip successfully.

The novel charge pump converter is designed for bulk process. To get high output the designed need to be changed for SOI process. In that case all PMOS need to be replaced y NMOS that will be another big challenge.