

Mohammad Rashedul Hoque

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OBJECTIVE

A challenging position in the field of analog and mixed-signal circuit design, layout and testing.

EDUCATION

Master of Science in Electrical Engineering, expected May 2003.

University of Arkansas, Fayetteville, Arkansas.

Current CGPA: **3.71**

RELEVANT COURSES:

Course	Grade
Integrated Circuit Design Lab I	A
Integrated Circuit Design Lab II	A
Electronic Packaging	B
Artificial Neural Network	A
Minicomputer Application	A
Modeling and Simulation of Mixed-Signal Circuits and Systems	B
Power switching converter	A
Analog IC design	Current Semester

Bachelor of Science in Electrical and Electronic Engineering, June 2000.

Bangladesh University of Engineering and Technology, Dhaka, Bangladesh.

CGPA: **3.67**

EXPERIENCE

Graduate Research Assistant, May 2001 – Present.

Mixed-Signal Computer Aided Design Laboratory

Department of Electrical Engineering, University of Arkansas

Designed and laid-out a high-voltage on-chip bias circuit for a microgyroscope that was used in micronavigation systems (a project funded by Jet Propulsion Laboratory). The chip designed consists of a power management and distribution (PMAD) section, a high voltage gyro bias section, a very low noise sigma-delta signal sense and processing section, and a digital core. The goal of this research is to design an on-chip DC-DC converter with high output voltage and pumping efficiency.

ENGINEERING PROJECTS

Digital IC Design Project- Jan 2002 to May 2002.

Designed, laid-out, and tested a 32-bit DNA matching chip for MOSIS 0.35 μ m C5N 5V process using Mentor Graphics IC design tools. The chip is capable of matching the sequence of amino acid in the DNA with a given library sequence.

Analog IC Design Project 1- May 2002 to June 2002.

Designed, laid out and LVS 18-stage Favrat charge pump circuit, which will produce 60 V at the output from a 3.3V supply. Several improvements have been made on conventional Favrat charge pump. SOI PMOS has back-gate effect for high voltage switching. Therefore, to achieve high output voltage NMOS body-diode has been implemented instead of PMOS switches. The circuit was laid-out for Honeywell Partially Depleted 0.35 μ m MOI5 3.3 V SOI RAD-HARD process.

Analog IC Design Project 2- December 2002.

Designed, simulated, and laid out a novel DC/DC converter to produce 15 V from a 5 V supply. The circuit is designed by combining Dickson and Favrat topologies. The circuit has 99% pumping efficiency and power efficiency around 70%. It is specifically designed for Tower Semiconductor 5 V, 0.5 μ m bulk process.

Die and IC testing- Feb 2002 to May 2002.

Designed and built a test-board to test 40-pin DIP Dickson charge pump chip. The die of the chip was primarily tested in the probe-station before it was packaged. The circuit is designed by using SOI NMOS body-diode instead of using conventional body diode to reduce the cut-in voltage. The circuit has been tested successfully and it produced 19.6 V from a 3.3 V supply.

VHDL-AMS Project- Jan 2002 to May 2002.

Developed a behavioral and circuit model of a "PLL-control Micro-strip Active Patch Antenna." programmable divider circuit of the PLL block controlled the oscillation frequency of the patch antenna.

COMPUTER SKILLS

Computers

PCs, Sun Workstations.

Operating Systems

Unix, Windows XP/2000/95/98/NT, DOS.

Programming

VHDL-AMS, C, Assembly Language.

Simulation tools

Mentor – Design Architect/ System Vision Pro, PSPICE, SPICE3, Saber, Cadence - Spectre.

Layout tools

Cadence – Virtuoso, Mantor – IC station.

Application

Autocad, QuickCam, Isolator, ExcelCam.

PUBLICATIONS

Mohammad R. Hoque, D. Moorman, T. McNutt, J. Zhang, T. Ahmad, T. Cao, A. Mantooth and M. Mojarradi, "High Voltage Dickson Charge Pump in an SOI Process" submitted to the *IEEE Transactions on Solid-State Circuits*, 2003.

REFERENCE

References are available upon request.

