A HIGH-FREQUENCY REVERSE-RECOVERY TEST CIRCUIT FOR THE CHARACTERIZATION OF SIC POWER DIODES

Kevin M. Speer, speer@uark.edu
Faculty Advisor: Dr. H. Alan Mantooth

ABSTRACT A high-speed reverse recovery test bed is constructed and tested, and its performance is validated based on comparison criteria determined by the prior completion of a similar test bed and its results.

BACKGROUND As most circuit simulators contain parts in their libraries corresponding to almost all commercially available silicon (Si) devices, presently there is no simulator in possession of a library part corresponding to any silicon carbide (SiC) devices.

The first step in obtaining these models, however, is to observe the electrical characteristics of the devices. Intricate test systems are developed device-specifically, and normally call for high voltage and/or high current capabilities, due to the high power performance benefits that SiC devices offer as compared to their Si counterparts.

WORK DONE The work summarized here consists of the construction of the reverse-recovery test bed previously used at NIST, and the evaluation of its performance on a comparison basis. The construction of the test bed is allowing the University of Arkansas to continue its success and build upon its world-renowned reputation of wide-bandgap semiconductor device modeling efforts, including experimentation involving devices; theoretical knowledge of wide-bandgap technology; and model design and implementation. The test bed consists of two basic parts: the high voltage power supply and the characteristic-specific test circuit.

The reverse recovery test bed requires a high-voltage power supply capable of delivering voltages of up to 600 V. Because the test bed is intended on observing the reverse recovery phenomena of the DUT, a high power supply output current is not necessary; provided that the regulatory output capacitance of the supply is capable of delivering periodic bursts of up to 700 mA (which is normally the maximum current level obtained in the circuit for testing SiC power diodes), meaningful and conclusive experimentation may be performed. Fig. 1 shows the schematic of the power supply constructed for use in the reverse recovery test bed.

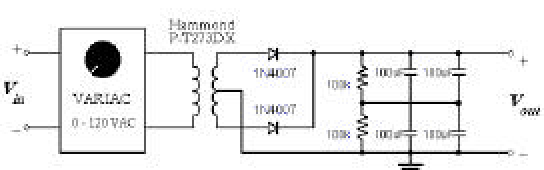

Fig. 1. Schematic for reverse recovery test bed power supply.

The circuit used for the characterization of the reverse recovery of diodes is shown in Fig. 2. When the MOSFET is on, the current flows through the transistor. As the MOSFET is switched off, the current flows through the device under test (DUT). When the MOSFET is switched back on, the transistor pulls the current from the DUT, thus forcing a negative current through the DUT. By pulsing the MOSFET five times, the inductor builds up stored energy and, on the fifth pulse, the most dramatic reverse recovery waveform is established and analyzed. The reason for pulsing the circuit is to reduce the system's thermal dependence and/or the occurrence of device overheating.

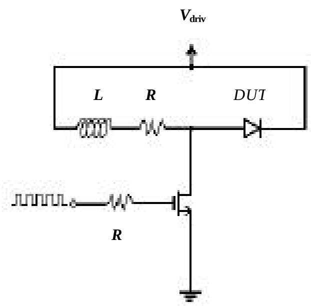

Fig. 2. Test Circuit schematic.

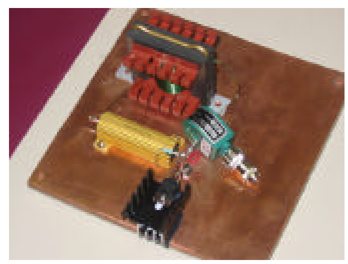

Fig. 3. Photograph of the test circuit.

RESULTS The test bed is demonstrated in Fig. 4, which shows the current and voltage waveforms measured with a V_{drive} of 250 V and a pulse rise time of approximately 23 ns. It is observed that as the voltage at the drain is reduced to zero (i.e., the MOSFET is switched on), the DUT current drops to a reverse peak of slightly larger than 600 mA, and eventually recovers to a zero value.

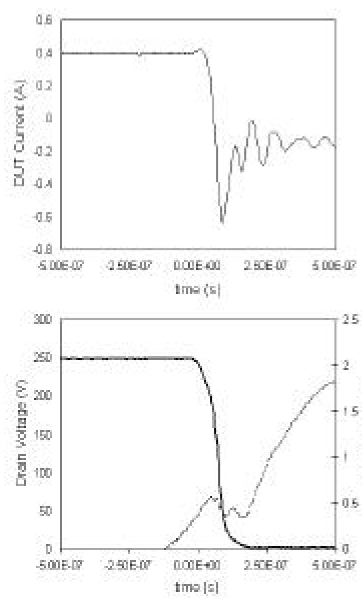

Fig. 4. (Top) Current through the DUT. (Bottom) Drain voltage (solid) and gate voltage (dashed) of the MOSFET.

FUTURE WORK We are beginning to implement SiC Static Induction Transistors (SIT) as the switch in place of the traditional MOSFET, in an effort to demonstrate the high-frequency superiority of SiC switching devices. A paper on this work was recently accepted for publication in the European Power Electronics conference, and the work will be presented in Toulouse on September 2-4, 2003.