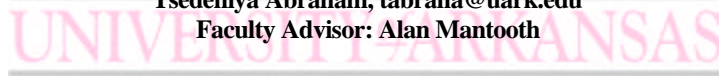


TWO STAGE OPERATIONAL AMPLIFIER

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OBJECTIVE The main objective of this project was to familiarize the student with the designing process and the trade-offs involved with circuit design.

The specifications for the design are indicated in the table below.

| Parameter | Value |
|-----------------------|-----------------|
| Voltage gain | 86.9dB |
| Power Supply | +/- 1.5 V |
| Slew Rate | +/- 0.33V/u sec |
| Out put voltage range | +/- 1.35V |
| PSRR (+) | 62.02dB |
| PSRR (-) | 61.47dB |
| CMRR | 104.1dB |

This is the internal circuitry of the amplifier designed.

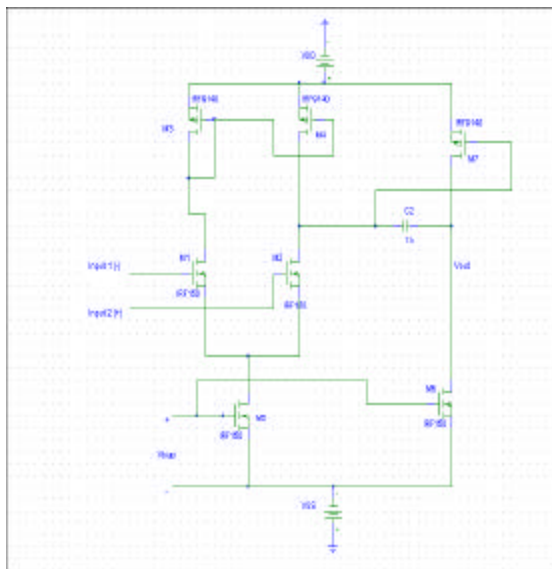


Figure 1. Schematic of the op-amp designed.

WORK DONE The design of the op amp was followed by simulation and layout. The first process used for fabrication is the Honeywell SOI5. While doing the layout for this process it became apparent that the length of the PMOS and NMOS devices was less than the minimum length allowed for this process. The next step was to redesign the op amp in a way that it would not violate the minimum length requirements.

| MOSFET | W/L ratio (um) |
|-----------|----------------|
| M1 and M2 | 0.6/2.85 |
| M3 and M4 | 0.6/3.15 |
| M5 | 0.6/3.2 |
| M6 | 0.6/4.9 |
| M7 | 0.6/3.10 |

The very next step was to redo the simulation in SABER The following table shows the results of the simulation.

| Parameter | Simulation results |
|----------------------|--------------------|
| Voltage gain | 50.12dB |
| Output voltage range | 1.26/-1.48 V |
| PSRR (+) | 49.442dB |
| PSRR (-) | 33.94dB |
| CMRR | 49.16dB |

After the layout was complete and all design rule checks were performed, the design was sent to fabrication. In the mean time a test plan was prepared.

FUTURE WORK After the chips get back from fabrication different tests will be performed in order to gather data and analyze its operation.