COMPACT CIRCUIT SIMULATION MODEL OF A SILICON CARBIDE VERTICAL JUNCTION FIELD EFFECT TRANSISTOR (V-JFET)

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ABSTRACT *A compact circuit simulation model is developed for a Silicon carbide (SiC) Junction Field Effect Transistor, used primarily as power switches. The MAST High Level language is used to model the transistor. The on-state and transient behavior of the model has been validated against measured data at 25°C and 100°C. This research work has been accepted for presentation at the IEEE Power Electronics Specialists Conference (PESC) 2004.*

BACKGROUND Silicon carbide (SiC) power devices are expected to show superior performance compared to other semiconductor materials primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and higher temperature capability than conventional Si materials. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices, the combination of 1/10th the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed.

Of all SiC power transistors (e.g., MOSFETs, JFETs, BJTs) currently under development, SiC JFETs have perhaps the greatest near term potential for commercialization for high temperature applications. The availability of compact circuit simulation models for these devices will greatly aid power electronics engineers in circuit design, testing, prototyping, and product development. This project aims at accurately describing the on-state and switching conditions of the SiC JFET (Fig. 1) over a wide range of application conditions and operating temperatures. These devices have a great commercial potential especially in the power, aero-space, communication and defense areas.

WORK COMPLETED A compact model has been developed for the SiC JFET. It was tested using the Saber simulator and validated with data characterized from devices provided by Northrop Grumman. As Fig. 2 above shows, there is an excellent agreement between the model and the measured data for the on-state waveforms. Switching transients have also been modeled and validated.

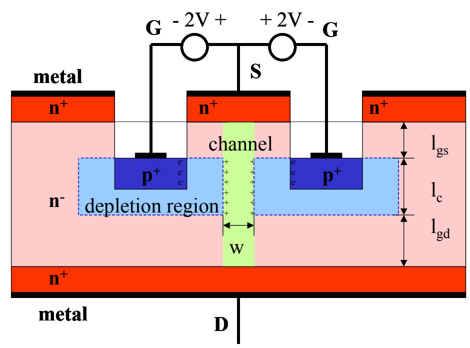

Fig. 1. Cross section of a Vertical Channel Junction Field Effect Transistor. The current flow is controlled by modulating the potential at the saddle point between the gate electrodes

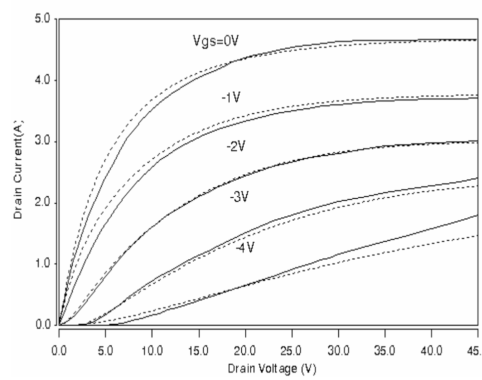

Fig. 2. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 25°C for different gate voltages.

REFERENCE

Kashyap A.S, Ramavarapu P.L, Maganlal S, McNutt T.R, Lostetter A.B, Mantooth H.A, "Modeling Vertical Channel Junction Field Effect Devices in Silicon Carbide", *Conf. Rec. of IEEE Power Electronics Specialists Conf (PESC)*, Aachen, Germany, June 20-25 2004.