

Chandrasekhar Vemulapally

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OBJECTIVE:

A challenging intern/co-op engineering position in the area of design automation, behavioral modeling and simulation, IC design, layout and Mixed-signal testing

SUMMARY:

- Proven ability to develop CAD tools and GUI applications in both Windows and UNIX environments
- In-depth knowledge of SPICE-level circuit simulation. Good understanding of simulation algorithms, model development process and parameters
- Thoroughly familiar with Cadence and Mentor design tools for schematic entry, SPICE and Spectre circuit simulations
- Experience in system-level behavioral modeling and simulation using VHDL-AMS, MAST and Verilog-A
- Good understanding of device physics, CMOS Design, IC (DRC and LVS) Layouts and Mixed-signal testing
- Ability to create scripts and automated procedures with knowledge of Object Oriented Programming/scripting in Python, XSL, XPath and C++ languages
- Strong commitment to learning, team work and ability to express both in verbal and written form

QUALIFICATION:

- **Ph.D.** student in Electrical Engineering
University of Arkansas, Fayetteville *(Expected Graduation: Dec, 2007)*
- **M.S.** in Electrical Engineering
University of Arkansas, Fayetteville (GPA - 3.7/4.0) *Jan 2002- Dec 2004*
- **B.E.** in Electronics and Communications Engineering
Karnatak University, India (GPA - 3.6/4.0) *Dec 1996 – Nov 2000*

EXPERIENCE:

Lynguent Inc., Fayetteville.

April 2005-present

Co-op Engineer (R & D)

- Ported Industry standard semiconductor device model **BSIMSOI 3.2**. in SPICE3f4 into the *ModLyng* environment
- Performed detailed analysis of the BSIM SPICE C code and translated the model from C to Verilog-A
- Validated the generated Verilog-A model in Cadence Spectre against the built-in SPICE model
- Support and maintenance of VHDL-AMS and MAST code generators
- Extended the Paragon modeling research tool to the commercial *ModLyng* version
- Assisted in Parameter extraction for semiconductor device models using ICCAP software

University of Arkansas, Fayetteville, AR

Research Assistant, Mixed-Signal Computer-Aided Design Lab

Jan 2002-April 2005

Modeling tools group

- Participated in the research, design and implementation of a new EDA environment called Paragon for creation, testing and validation of HDL-based behavioral models
- Developed automatic Code generation modules for generating analog and mixed-technology models in **VHDL-AMS** and **MAST**
- Implemented AST algorithms for avoiding unnecessary iterations and generating fast and efficient code
- Modeling/Simulation of semiconductor device models like **EKV 2.6 MOSFET** and **SiC JFET** models
- Writing Regression test suites for testing models in the Model library
- Automatic Code generation for SPICE-like simulator called **VTB** developed at the University of South Carolina
- **Design, simulation** and **layout** of a 32-bit DNA pattern-matching chip using Mentor Graphics IC design tools

EDC Lab, Karnatak University, India.

Technical Lab Assistant

Feb-Oct 2001

- Worked in the Electronic devices and circuits lab for undergraduate students. Helped in setting up experiments and analyzing the characteristics of various devices and digital logic.

COMPUTER SKILLS:

Programming/Scripting: Python, sed, PyQt (GUI applications), C, C++, FORTRAN and MATLAB.

Markup Languages: XML, Xpath and XSL.

Assembly languages: Microprocessor 8085 and 8086.

Hardware description languages: VHDL, VHDL-AMS, MAST and Verilog-A.

CAD Tools: Mentor Graphics (IC Station, QuickSimII, Design Architect), Analog Artist, Spectre (Cadence) PSPICE, SPICE 3f4, ORCAD, Dymola (Dynasim), System Vision (Mentor Graphics), Active-HDL (Aldec), VeriasHDL, SABER (Synopsys), Qt Designer and working knowledge of version control system.

PROJECTS:

Mixed-Signal Testing

Jan-April 2005

Studied the basic techniques required in testing of DAC and ADCs. Implemented Major Carrier Testing for an 8-bit ADC from TI and compared against the theoretical values. Various intrinsic and extrinsic parameters were discussed for the data converters.

CAD Methods for VLSI

Aug-Dec 2003

Rather than using ROBDDs, an algorithm was developed to test the equivalence of given SOP expressions using a software module. Famous algorithms used in VLSI CAD applications were implemented.

CMOS analog circuit Design

Jan-April 2003

Design and Simulation of CMOS analog circuits using PSPICE. Fundamental and complex circuits with CMOS Operational amplifiers and their characteristics (for common-mode and differential) were simulated. Important design aspects like Aspect ratio, Slew rate, Gain, Noise analysis, Feedbacks, etc. were considered.

Design of MIPS architecture

Aug-Dec 2002

Design of *data path* and *control* of the MIPS architecture was simulated using Mentor Graphics design suite. Architecture was validated for 32 bit instructions.

Modeling and Simulation of Mixed-Signal circuits and systems

Jan-April 2002

A top level behavioral model of an Analog Oscilloscope was implemented focusing on the triggered sweep and 555 timer using VHDL-AMS. Both behavioral and circuit level models were simulated and compared in System Vision.

PUBLICATIONS:

Y. Chernukhin, M. Polenov, **C. Vemulapally**, E. Solodovnik, H.A. Mantooth, R. Dougal, "Deploying Modelica Models into Multiple Simulation Environments," *IEEE International Workshop on Behavioral Modeling and Simulation BMAS 2005, San Jose, CA, Sep 22-23, 2005*.

A. S. Kashyap, **C. Vemulapally**, H. A. Mantooth, "VHDL-AMS Modeling of Silicon Carbide Power Semiconductor Devices," *IEEE Workshop on Computers in Power Electronics (COMPEL)*, Urbana Champaign, pp. 50-54, Aug 2004.

P. Mallick, M. Francis, **C. Vemulapally**, A. Austin, H. A. Mantooth, "Achieving language independence with Paragon," *International Workshop on Behavioral Modeling and Simulation (BMAS)*, pp. 149-153, Oct. 2003.

COURSE WORK:

Analog Integrated Circuit Design

Mixed-Signal Testing I and II

Modeling and Simulation of Analog and Mixed-Signal systems

Integrated Circuit Design I and II

Power Electronics

Introduction to Computer Architecture

Digital Electronics

CAD Methods for VLSI

Semiconductor Devices

Software Engineering

IC Fabrication Technology

Microprocessors (8085 & 86)

Digital Signal Processing

Pulse and Switching Circuits

REFERENCES:

Available upon request.
