

Identification and Modeling of Nonlinear Dynamical Behavior in Analog Circuits

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ABSTRACT There are two contributions of this work: 1) a technique for identifying nonlinear dynamical behavior in analog circuits was developed and 2) a tool for fully automatic behavioral model generation of nonlinear analog circuits was implemented.

BACKGROUND The growing complexity of analog and mixed-signal systems continues to stimulate the need for behavioral models of analog components. Behavioral models are used both for top-down design and for bottom-up verification. While things have matured nicely in the modeling of linear circuits and systems, the present methodologies for nonlinear circuit modeling are circuit-specific. Developing modeling methodologies for circuits with strong nonlinearities remains a challenge, since deep insight into nonlinear dynamical circuit behavior is necessary. The objective of this project is to research and develop algorithms and tools for the generation of HDL-based behavioral models for nonlinear circuits.

APPROACH The behavioral modeling tool (Fig.1) starts from the netlist description of the circuit and generates differential algebraic equation (DAE) based behavioral models. It is a *bottom-up* behavioral modeling approach that does not require a pre-defined template. The basic idea behind this approach is to analyze the original circuit for a) signal path information, b) linear frequency response, and c) nonlinear time-domain response to identify a subset of nodes in the original circuit. Each node is physically represented by a collection of elements such as voltage-controlled current sources and linear and nonlinear passives. Kirchhoff's Current Law (KCL) is applied to these nodes to derive a reduced set of DAEs that represent the behavioral model.

WORK DONE This behavioral modeling method has been fully automated in the behavioral modeling environment PARAGON. PARAGON was designed to create behavioral models in multiple hardware description languages (HDLs). The model can be generated in any hardware description

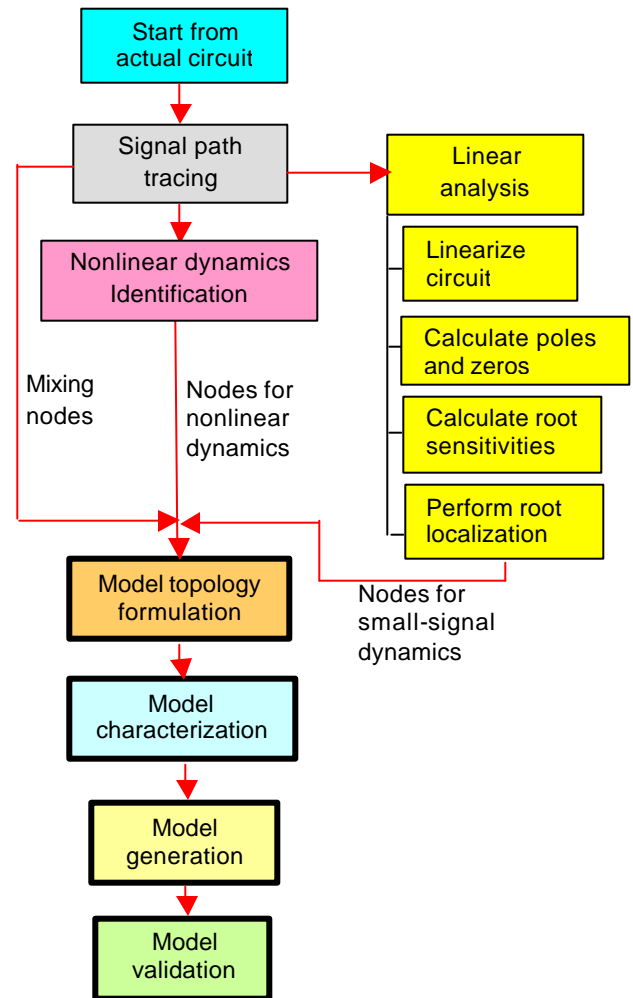


Fig. 1 Modeling Procedure

language such as MAST or VHDL-AMS. A friendly user interface is implemented, guiding modelers through the step-by-step model generation and characterization process. Simulation times for the models compare quite favorably to those of the original circuits (> 10x improvement typical), while high degrees of accuracy are maintained.