THE MODELING ENVIRONMENT -- PARAGON

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ABSTRACT A mixed signal behavioral modeling environment for the creation, testing and validation of HDL-based models is presented. The environment is designed to support the generation of multiple hardware description languages.

BACKGROUND Hardware Description Languages (HDLs) have become a vital part of most digital design flows. They are being employed in an ever-increasing fashion for analog and mixed-signal circuits and systems. However, the language technology alone is insufficient to promote widespread use of HDLs by the design community. Even with the use of state-of-the-art simulation and modeling tools, complex designs can take weeks and even months of simulation and modeling work before all the relevant aspects of the design are successfully simulated. Most designers approach a simulator with the goal of observing the operation of a particular design.

APPROACH Paragon was designed to create behavioral models in multiple hardware description languages. The concept was to provide a modeling environment that frees the model developer from the need to learn multiple languages. The behavioral models in multiple hardware languages were created using a centralized database. This database contained all the relevant information about the model in a language independent format.

The modeling environment of Paragon includes three parts: model creation, model robustness, and model testing and validation. It enables the designer or model supplier to more quickly create new models, reuse parts of existing models, and develop through model test and validation procedures. The quality of models is improved through model robustness tools, which enable the model developer to analyze properties of the model and specify model-based simulation algorithm controls. A big advantage of Paragon is that it produces readable, standardized code that captures design intent and removes the common errors that cause unnecessary iterations.

The model creation capabilities of Paragon culminate in the code generation tool. It consists of several interfaces that can operate on the same document.

WORK DONE Now the model can be generated in hardware description languages such as MAST or VHDL-AMS. A friendly user interface is implemented, guiding modelers through the step-by-step model generation and characterization process.

FUTURE WORK Use the DAE (Differential Algebraic Equation) and DDD (Determinant Decision Diagram) methods to test and validate the model.