

Paragon – A Mixed-Signal Behavioral Modeling Environment

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ABSTRACT This work involves the development of a mixed-signal behavioral modeling environment for the creation and validation of hardware description language based models. The environment presently supports the generation of multiple hardware description languages including VHDL-AMS and VTB.

BACKGROUND Hardware Description Languages (HDLs) have become a vital part of most digital design flows. They are being employed in an ever-increasing fashion for analog and mixed-signal circuits and systems. However, analog designers are not as inclined to write programs as part of their design activity. They tend to work and think more graphically than digital designers, who themselves employ VHDL or Verilog, synthesis, and place-and-route tools. Language-based design tools, which provide graphical user interfaces in addition to textual, are one means of addressing this barrier to use. This is only now becoming the case for analog or mixed-signal designs. The main objective of this modeling tool research is to streamline the process of creating analog and mixed-signal behavioral models from various sources.

WORK DONE The software architecture of Paragon has been described through a system block diagram shown in Fig. 1. This figure shows the major modules that comprise Paragon. The interconnections between the modules are intended to convey flow in the use of the modules, as they would be encountered in the modeling process.

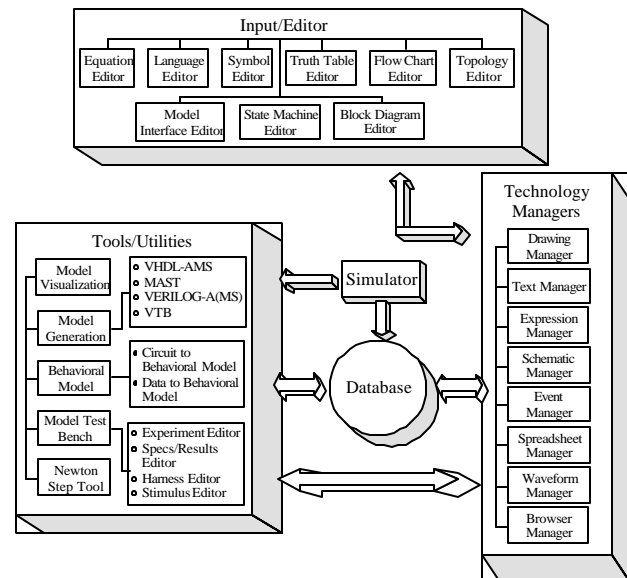


Figure 1: System block diagram of Paragon indicating the major functional modules.

The model creation capabilities of Paragon culminate in the code generation tool. The XML description of the model can be stored and version-controlled, so that changes can be reflected in models of all downstream HDLs. By defining a consistent, implementable set of semantics that is independent of any particular HDL, Paragon is capable of generating models in various HDLs. Thus, by using Paragon, an analog designer can create models in multiple HDLs, without knowing or learning any of them.

FUTURE WORK One of the major future works is to add code generation capabilities in more HDLs, like Verilog – A(MS) and MAST. Also, another work is to generate code for models in the C language that can be simulated in simulators like MICA, Spectre and HSIM.