HIGH VOLTAGE DC-DC CONVERTER USING POST-PROCESSED INTEGRATED CAPACITOR TECHNOLOGY ON SOI

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ABSTRACT - In this work, a high-voltage, on-chip DC-DC converter based on voltage doubler technology is designed. The circuit as originally designed for bulk CMOS, is modified for a Silicon-On-Insulator (SOI) CMOS process. Integrated capacitor technology is subsequently deposited directly onto the completed wafers to improve the efficiency and output ripple of the charge pump while keeping the area of the chip from increasing. The design of a 3.3-V input to 30-V, 44-µA output DC-DC converter is presented as design specification.

BACKGROUND - A charge pump is a dc-dc converter that uses only capacitors for storing energy. Using only capacitors, which takes less area than inductors in an integrated circuit, allows charge pump circuits to be fully integrated. Smaller and more efficient charge pump is desired for portable devices.

A new topology based on the Dickson charge pump, Favrat charge pump, is originated for bulk CMOS process. This topology needs to be modified for SOI CMOS process. The advantage of SOI is that it has less parasitic junction capacitance.

The Favrat charge pump is more efficient with smaller output ripple voltage. Unlike the Dickson charge pump that only uses one booster circuit and one pass gate transistor, the Favrat charge pump uses two booster circuits and two pass gate transistors. First pass gate transistor conducts during the first half, while the second conducts during the second half of a clock cycle. Another advantage of the Favrat charge pump compared to the Dickson charge pump is that the booster circuit is configured in such a way that the boosted signals do not suffer from the voltage loss due to the threshold voltage of the transistors.

The design of a 3.3-V input to 30-V, 0.1-V ripple, 44-µA output DC-DC converter is decided to be a design specification. The project also focuses on the post-process integrated capacitor. Post-processed integrated capacitor technology can be employed to improve the efficiency of the converter without sacrificing chip's area.

WORK DONE - The original Favrat is modified to solve the back channel effect in SOI process. PMOS switches could possibly not be turned off because of the back channel devices. The pass gate transistors are then replaced with diode connected NMOS transistors. This configuration is projected to have less threshold voltage than regular diode, which helps in the improvement of the efficiency of the charge pump. The modified circuit is shown in Fig. 1.

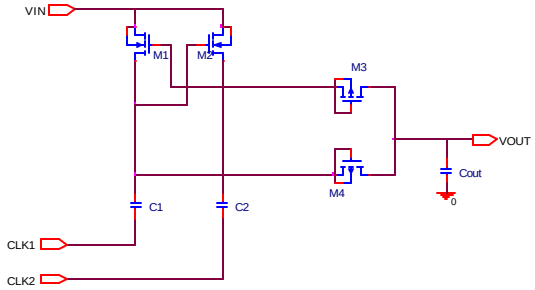

Fig. 1. Favrat Charge Pump for SOI Process

Several designs have been sent for fabrication. Some of them are designed to have probe pads for contacting the post-process integrated capacitor.

To meet the specification, 15 stages of charge pump are constructed. The simulation result is shown in Fig. 2.

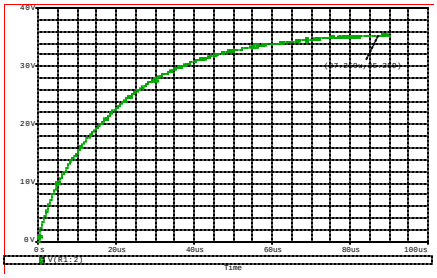

Fig. 2. Simulation Result

RESULTS - The advantage of SOI CMOS process for charge pump chip fabrication is realized. It has less junction parasitic capacitance and the diode connected NMOS which can be implemented only in SOI causes less voltage drop at the output.

FUTURE WORK - The next challenge is the inclusion of the post-process integrated capacitors and test the fabricated chip.