

## Alexander B. Lostetter, Ph.D.

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- Objective** A position in power electronics and/or microelectronics packaging R&D.
- Education**
- Ph.D. in Microelectronics-Photonics, January 2003 GPA: 3.95 / 4.0 Overall  
 University of Arkansas, Fayetteville, AR.  
 Dissertation: *The Design, Fabrication, and Analysis of Half-Bridge Multichip Power Modules (MCPMs) Utilizing Advanced Laminate, Silicon-Carbide, and Diamond-Like-Carbon Technologies.*
- M.S. in Electrical Engineering, May 1998 GPA: 3.8 / 4.0 Overall  
 Virginia Polytechnic Institute & State University, VA.  
 Thesis: *Miniaturization, Packaging, and Thermal Analysis of Power Electronics Modules*
- B.S. in Electrical Engineering, August 1996  
 Virginia Polytechnic Institute & State University, VA.
- Employment**
- 11/99-Present COO / Design Engineer, Arkansas Power Electronics International, Inc.  
 700 Research Center Blvd, Fayetteville, AR.
- Promoted from design engineer to COO and full partner in December 2001. APEI is currently a small business with 5 employees and an average of 3 subcontractors.
  - Responsible for leading technical operations in power electronics design, fabrication, packaging, and testing, including high temperature electronics and SiC power device applications.
  - Responsible for funding/proposal submissions for small business research grants, interfacing with customers, and promoting/marketing business ideas. Contracts have included redesign work for the U.S. Air Force F-15's generator control unit and high temperature power electronics design for down-hole logging tools.
- 10/02-Present Post Doctoral Researcher, Silicon-Carbide (SiC) Device Modeling Group  
 University of Arkansas, Fayetteville, AR.
- Responsible for technical lead and management of the group with approximately 10 Ph.D., M.S., and undergraduate students.
  - Modeling and parameter validation of experimental prototype SiC electronic devices under development by industry leaders, such as Cree and Northrop Grumman. Includes high-level hardware description language programming (MAST) and the design and building of device characterization test circuits. Devices currently under test include Cree SiC Schottky diodes and power MOSFETs, and Northrop Grumman SiC static-induction-transistors (SITs).
- 9/99-8/02 Graduate Research Assistant, Mixed-Power Electronics Laboratory  
 University of Arkansas, Fayetteville, AR.
- Design, miniaturization, modeling, and packaging of power electronics utilizing diamond-like carbon (DLC), SiC devices, low-cost flexible polyimide substrates, bare-die, direct bond copper (DBC), ceramics, integrated passives, and thick-films.
  - Design and analysis of CMOS thermal transducers for data isolation in NASA JPL's systems on a chip (SoC) deep-space program.
  - Project manager and team leader of College of Engineering Solar-Electric Boat Program, including management of 30 students with a \$20,000 per year budget (1/10<sup>th</sup> the budget of

main competitors). The UA captured the 2002 World Championship against ~25 international teams: refer to [www.uasolarboat.com](http://www.uasolarboat.com) or [www.solarplash.com](http://www.solarplash.com).

- 1/97-8/99 Graduate Research Assistant, Microelectronics Laboratory  
Virginia Tech, Blacksburg, VA.
- Design, miniaturization, and packaging of low cost and high performance power electronic converters, including thermal and stress analysis, modeling, simulation, and experimentation.
- 5/98-9/98 Intern, Lockheed Martin Federal Systems, Semiconductor Device Technology Center (Space Electronics Division), 9500 Godwin Dr., Manassas, VA.
- Reliability and failure analysis engineer subcontracted to Lockheed by Va. Tech.
  - Performed thermal-stress computer modeling (ANSYS™) and experimental analysis on failed space radiation-hardened semiconductor devices and packages.
  - Investigated the space radiation-hardened semiconductor fabrication process line for issues and problems which translated to final product reliability concerns.
- 11/95-12/96 Undergraduate Research Assistant, Microelectronics Laboratory  
Virginia Tech, Blacksburg, VA.
- Fabricated microelectronic packages utilizing PCB, thick film, and LTCC technology.
  - Evaluated electronic designs through Saber and PSPICE computer simulations.

### Teaching

- 1/00-Present Instructor, University of Arkansas, Fayetteville, AR.
- Instructed sophomore & junior level circuits and electronics lecture courses including Electric Circuits I, Electric Circuits II, and Engineering Electronics.
- 1/97-12/98 Instructor, Virginia Tech, Blacksburg, VA.
- Instructed senior level Microelectronics Design lecture course and senior level Microelectronics Laboratory course covering topics including, thick and thin film circuit design and fabrication, LTCC processing, PCB processing, MCM design, electronic packaging techniques, and reflow solder and die attach methods.

<b>Advanced Courses</b>	Microelectronics Design	Microwave Packaging	Radio Engineering
	Power Electronics Design	Advanced Packaging I&II	A/D Communications
	Electronic Circuits Design	Power Packaging	Fiber Optics
	RC Active Filter Design	Semiconductor Devices I&II	Management Operations
	IC Design & Lab	High Speed Devices	Micro-EP Operations
	IC Fabrication Processes	Entrepreneurial Management	

**Computer Skills** Pspice, Orcad, FLOTHERM™, FLOSTRESS™, ANSYS™, Saber, Mentor, Eclipse, Design Star, Encore MCM (Finesse), Mathcad, Autocad, BASIC, and Fortran.

**Laboratory** Extensive knowledge and experience with metallization etching techniques and PCB manufacturing, computer design and mask generation, electroplating (nickel, gold, and copper), thick film printing and LTCC, furnace firing operations, reflow solder operations (SMD and bare die devices), laser cutting operations, circuit testing, wire bonding techniques, high temperature polymer bonding, polymer flex circuitry, polymer thick films, direct bond copper (DBC), and diamond-like carbon (DLC) substrates. Some experience with thin film deposition techniques and thin film masking procedures.

### Organizations

- 9/00 – 8/02 Project Manager of UA College of Engineering Solar-Electric Boat Program.  
4/96 – 8/98 Vice-President of Virginia Tech Student Chapter of IMAPS (ISHM).

- 2/96 – Present Member of Eta Kappa Nu (Electrical Engineering Honor Society).  
 11/95 – Present Member of IMAPS.  
 11/95 – Present Member of IEEE.

### Awards

- 5/02 Awarded 1<sup>st</sup> place University of Arkansas Graduate Researcher for 2001-2002.  
 6/01 Awarded 2001 NSF-IGERT Summer Travel Program
- Spent 3 months in summer of 2001 visiting universities and companies (in 12 European countries) that perform research in the areas of power electronics and power electronic packaging.
  - Duties included exchange of ideas with hosts, presenting research seminars, and recruiting students for UA engineering and sciences graduate programs.
- 1/00 Awarded W.R. Thomas Doctoral Fellowship (per semester, 4 years).  
 8/99 Awarded National Science Foundation IGERT Fellowship (per semester, 3 years).  
 8/99 Awarded University of Arkansas Doctoral Fellowship (per semester, 4 years).  
 11/98 Awarded Philips Electronics 98-99 Graduate Research Fellowship.  
 8/98 Awarded IMAPS 98-99 Educational Foundation Research Grant.  
 10/97 Awarded best student conference paper AND best paper of session of IMAPS '97 International Conference.  
 8/97 Awarded IMAPS 97-98 Educational Foundation Research Grant.

### Publications

- Advanced Electronic Packaging, 2<sup>nd</sup> Edition (Chapter 13: Power Electronics Packaging), Edited by Dr. W. Brown, IEEE Press (Textbook— accepted but not yet in print).
- *Testing Electrical Characteristics of Novel Silicon Carbide Static-Induction-Transistors (SITs) for use in High-Temperature Packaging Applications*, IMAPS 2003 International Symposium on Microelectronics, Boston MA. (Submitted, not yet accepted).
- *A Novel High Frequency Silicon Carbide SIT-Based Test Bed for the Acquisition of SiC Power Device Reverse Recovery Characteristics*, 2003 European Power Electronics Conference, Toulouse France (Accepted, not yet published).
- *An SOI CMOS Compatible Thermal Transducer for Low Power Systems on a Chip (SoC) Data Isolation*, IEEE Electron Device Letters (Submitted, not yet accepted).
- *Novel Silicon-Carbide (SiC) Based Semiconductor Transistors for Use in High Temperature Power Electronics Packaging*, UA 2002 Technical Summit Conference, Fayetteville, AR, April 2002.
- *A Novel SOI CMOS Compatible Thermal Device Technology*, THERMES 2002, January 2002, California.
- *Silicon Carbide Power Die Packaging in Diamond Substrate Multichip Power Module Applications*, 2001 IMAPS Conference, Baltimore.
- *The Utilization of Diamond and Diamond-Like Carbon Substrates for High-Performance Power Electronic Packaging Applications*, 2001 European Power Electronics Conference, Graz, Austria.
- *Packaging of Polymer Thick Films (PTF) on Flex Substrate Power Converters*, IEEEPEP 2000 Conference on Power Electronics Packaging, Boston, July 2000.
- *The Utilization of Polymer Thick Film (PTF) and Flex Technologies for Power Electronic Packaging*, Proceedings of the 2000 International Symposium on Microelectronics and Packaging, Israel, June 2000.
- *The Utilization of Polymer Thick Film (PTF) and Flex Technologies for Low Cost, High Performance Power Electronics Packaging of a DC/DC Down Converter*, IMAPS 1999 International Symposium on Microelectronics, Chicago, November 1999.
- *An Overview to Integrated Power Module (IPM) Design for Power Electronics Packaging*, Journal of Microelectronics Reliability, pp365-379, September 1999 (Invited Paper).
- *Integrated Power Modules (IPMs), A Novel MCM Approach to High Power Electronics Design and Packaging*, The International Journal of Microcircuits & Electronic Packaging, Vol. 21, No.3, pp.274-278, 3<sup>rd</sup> Quarter 1998.
- *Multilayer Interconnects for a High Power Packaging Strategy*, IMAPS 1998 International Symposium on Microelectronics, San Diego, pp.330-334, November 1998.
- *Packaging and Thermal Analysis of High Density Power Modules*, Proceedings of the 1998 International Symposium on Microelectronics and Packaging, Israel, pp.92-99, June, 1998.
- *Thermal Evaluation and Comparison Study of Power Baseplate Materials*, Advancing Microelectronics, Vol.25, No.1, pp.25-27, January/February 1998.
- *High Density Power Modules: A Packaging Strategy*, IMAPS 1997 International Symposium on Microelectronics, Philadelphia, pp.102-107, October 1997 (Best paper of session, Best student paper of conference).
- *Thermal Management and Materials Issues for Multichip Power Electronics Modules*, Advanced Technology Workshop (ATW) on Advancements in Design, Materials, and Processes for Thermal Spreaders and Heat Sinks, April 1997.
- *Electronic Packaging for Power Electronic Building Blocks*, GOMAC, pp.433-436, March 1997.
- *Materials Issues for Solutions of Power Electronic Building Blocks (PEBB)*, International Symposium on Advanced Packaging Materials, March 1997.