

AVINASH S. KASHYAP

55 S. Razorback Rd, Apt #9

Fayetteville, AR 72701

Phone: Cell- (479)236-0280; Office-(479)575-3295; Home-(479)521-6633

Email: akashya@uark.edu

Personal Home page: <http://comp.uark.edu/~akashya>

Lab URL: <http://mixedsignal.eleg.uark.edu>

OBJECTIVE:

Seeking a challenging, research oriented position in semiconductor design, modeling or testing.

EDUCATION:

M.S. Electrical Engineering, Dec 2004

*University of Arkansas, Fayetteville. GPA: 3.8

*Thesis: *Compact circuit simulation modeling of silicon carbide vertical channel junction field effect devices.*

*Relevant coursework-taken: Mixed signal test engineering, Mixed signal modeling & simulation, IC design & layout (Analog & Digital), Advanced IC fabrication technology, Semiconductor devices, High speed semiconductor devices, Power electronics.

B.S. Electrical & Electronics Engineering, June 2001 (On a full merit scholarship awarded by the State Government of Kerala)

*University of Calicut, India. Equivalent GPA: 4.0

*Ranked first in EEE Dept. Class of 2001 among 98 students.

EXPERIENCE:

Jan2003-Present:

Graduate Research Assistant: Mixed Signal CAD Lab, University of Arkansas, Fayetteville, under Dr. Alan Mantooth.

Compact circuit simulation modeling of a Silicon Carbide Static Induction Transistor (SIT) and JFET, using the MAST High level modeling language and simulating it using the SABER suite. The work involves developing models for power switching applications. The devices have also been modeled in VHDL-AMS using the PARAGON package developed in-house. The model has been validated with actual device measurements. It is a NSF funded project in collaboration with NIST, Northrop-Grumman, NASA Glenn and Cree Research. This will be the first ever-developed unified simulation model for a SiC SIT and JFET. The research work has been accepted for presentation at the Power Electronics Specialists Conference 2004 at Aachen, Germany and other conferences.

July2001-June 2002

Research Intern: Institute of Microelectronics, Science Park II, Singapore.

On invitation by the Government of Singapore to attract talented students from Asia to live and work there. One of the 6 selected students from a total applicant pool of 1200. Was involved in a project to model an RF power MOSFET used in cell phone base stations for Oki Semiconductor Corp., Japan. The work involved device parameter measurements, calculations based on device physics and design of 20W Class-D power amplifier. Have also extensively worked in Class 100/10 clean rooms, operating all the relevant equipment and software.

June 2000-March 2001

Teaching Assistant: Electrical & Electronics Engineering Dept., University of Calicut India. Was an instructor for electric circuit theory and device electronics for sophomore students.

April 1999- June 1999

Summer Intern: Apollo Hospitals, Chennai, India

Was involved in the study of Medical Electronics and Diagnostic equipment in one of the world's largest corporate hospitals. Also gave a report to the management on future needs, equipment maintenance and industry trends.

ACADEMIC PROJECTS:

- i) **Mixed Signal Test Engineering:** Mixed Signal testing of various ICs using the techniques outlined in the book "Introduction to Mixed signal IC test and measurement", a Texas Instruments sponsored book.
- ii) **VLSI design:** Layout of 32 bit serial multiplier and 32 bit DNA string matching chip using the Mentor IC suite. Layout sent to MOSIS for fabrication. Used complete Mentor suite including Design Architect, QuickSimII, IC Station etc.
- iii) **Mixed signal modeling:** Model of a MEMS switch and micro-stepper motor assembly.
- iv) **IC Fabrication:** Deep Reactive Ion Etching of high aspect ratio Vias and their characterization.

COMPUTER SKILL SET:

Honors Diploma in Networked Centered Computing from the National Institute of Information Technology (NIIT) - Feb 2000

Operating Systems: Windows, DOS, Unix

Languages: C++, FORTRAN, MAST, VHDL-AMS, Assembly language (8085 & 8086)

Packages: SABER (Synopsys), Pspice (OrCAD), System Vision (Mentor Graphics), Simplorer (Ansoft)

T-Suprem4, ICCAP, MEDICI, Mentor Graphics IC design station, Verias HDL

Professional Suites: MS-Office

RDBMS : Sybase, MS-ACCESS

Quality Management : ISO, SEI CMM, Software Engineering

LABORATORY EXPERIENCE:

Teradyne ATE tester, Assesi probe station, HP Parameter Analyzer (4156A), HP Precision LCR meter (4284A), Optiprobe, Focused Ion Beam Equipment, Scanning electron microscope (Hitachi), MBE & CVD equipment

LANGUAGES KNOWN:

English, French, German, Tamil, Hindi, Malayalam, Sanskrit

AWARDS & ACCOLADES:

*Was awarded the State Government of Kerala Merit scholarship for academic excellence. Undergraduate tuition and expenses were fully sponsored by the Government.

*Ranked First in EE Department in College, Class of 2001. Selected as the Best Outgoing student in college.

*Was placed in the top 0.2% among 57,000 students in the Kerala State Engineering Entrance Examination.

*Unanimously elected as the President of the Electrical Engineering association in college, representing a student body in excess of 400.

*Authored numerous award winning research and review papers, both in undergraduate and graduate levels.

ORGANIZATIONS:

* Institute of Electrical and Electronics Engineers (IEEE)

* IEEE Communications Society (COMSOC)

* International Microelectronics and Packaging Society (IMAPS)

* IEEE Components, Packaging, and Manufacturing Technology (CPMT)

SELECTED PUBLICATIONS:

***Kashyap A.S.**, Ramavarapu P.L, Maganlal S , McNutt T.R, Lostetter A.B, Mantooth H.A, "Modeling Vertical Channel Junction Field Effect Devices in Silicon Carbide", *Conf. Rec. of IEEE Power Electronics Specialists Conf (PESC)*, Aachen, Germany, June 20-25 2004.

***Kashyap A.S.**, Mantooth H.A, "Compact Circuit Simulation Model of a Silicon Carbide Junction Field Effect Transistor", *IEEE Workshop on Computers in Power Electronics (COMPEL '04)*, Urbana-Champaign, Aug 15-18 2004. Submitted.

***Kashyap A.S.**, Vemulapally C, Mantooth H.A, "VHDL-AMS Modeling of Silicon Carbide Power Semiconductor Devices", *IEEE Workshop on Computers in Power Electronics (COMPEL '04)*, Urbana-Champaign, Aug 15-18 2004. Submitted.

***Avinash S. Kashyap**, Sharmila D. Magan Lal, Ty R. McNutt, Alexander B. Lostetter & Alan H. Mantooth "Testing and Modeling Electrical Characteristics of Novel Silicon Carbide (SiC) Static Induction Transistors (SITs)", Proceedings of the Arkansas Tech Summit, April 2003.

***Avinash S. Kashyap**, Sharmila D. Magan Lal, Ty R. McNutt, Alexander B. Lostetter & Alan H. Mantooth "Testing and Modeling Electrical Characteristics of Novel Silicon Carbide (SiC) Static Induction Transistors (SITs)", Journal of the Arkansas Academy of Sciences, April 2003.

***Avinash Kashyap**, "Feasibility Study of Global Positioning Systems for developing Countries", *Kaleidoscope, IEEE Annual Student Congress of Kerala section*, held in Government Engineering College, Thrissur, University of Calicut, Kerala. August 1999. 2nd prize in the paper presentation competition.

***Avinash S Kashyap**, "Hybrid Fuel Cell Gas Turbine Power Plant, with quasi zero emissions utilizing Sewage gas", *National Renewable Energy Conference 2000(NREC 2K)*, Indian Institute of Technology, Bombay, Nov 30 – Dec 2, 2000. Paper published as part of the Proceedings of the Conference.

*Above paper also presented in Indian Institute of Technology, Madras, in their *National Tech Fest, "Sbaastra 2K"*, March 2000. (The design was suggested to be a prospective one for a Patent).

INTERESTS:

Device Modeling, IC Layout, IC design, IC Fabrication/Processing, Testing, Material science

REFERENCES:

Dr. Alan Mantooth
Director, MSCAD Lab,
University of Arkansas
3217 Bell Engineering Center
Fayetteville, AR 72701
E-mail: mantooth@enr.uark.edu
Phone: (479) 575-4838
Fax: (479) 575-7967

Dr. Aicha Elshabini
Distinguished Professor & Head
Dept. of Electrical Engineering
University of Arkansas
Fayetteville, AR 72701
E-mail: aicha@enr.uark.edu
Phone: (479) 575-3009
Fax: (479) 575-7967
