A Novel High Frequency Silicon Carbide Static Induction Transistor-Based Test-Bed for the Acquisition of SiC Power Device Reverse Recovery Characteristics

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Abstract– A test system is presented that utilizes a high-frequency Silicon Carbide (SiC) Static Induction Transistor (SIT) in place of the traditional MOSFET to test reverse recovery characteristics for the new class of SiC power diodes. An easily implementable drive circuit is presented that can drive the high-frequency SIT. The SiC SIT is also compared to a commonly used Si MOSFET in the test circuit application.

I. INTRODUCTION

In this paper, a high-speed reverse recovery test system is developed that offers ease of implementation and well-characterized components and parasitic phenomena. The system is specifically designed for the characterization of high-speed SiC power diodes; this characterization is done by emulating a wide range of application conditions by independently controlling the applied diode voltage, forward diode current, di_D/dt, and dv_D/dt at turn-off. By emulating such a wide range of application conditions, the system is very useful in characterizing the power diode's forward and reverse recovery phenomena, thus providing a controlled environment of known parameters for conducting parameter extraction for compact model development. The system further demonstrates its value by providing a means of model validation, the final step in model development [1].

SiC PiN diodes have demonstrated reverse recovery times of 6 ns [2, 3], and the SiC Schottky and Merged Pin Schottky (MPS) rectifiers have demonstrated even faster switching times than PiN rectifiers due to the unipolar nature of their operation range [4]. Because the SiC diodes are orders of magnitude faster than comparable Si diodes, a new test circuit was developed that can stress the SiC diodes [2]; as such, the SIT is a noteworthy candidate for the semiconductor switch in the high-speed reverse recovery test circuit shown in Fig. 1. The SIT has a lower parasitic capacitance and a faster switching speed than the conventionally-utilized power MOSFET. The primary factor in using a SIT is the aforementioned increase in switching speed; however, another amenity is the SIT's superior voltage blocking capability that legitimizes its use in high power applications, making it an ideal switch for SiC diodes.

II. STATIC INDUCTION TRANSISTOR OPERATION

SIT Structure

Fig. 2 illustrates the structure of the SIT. In this work, the SIT is operated in its unipolar region of operation (i.e., the gate p-n junctions do not become forward biased). Unlike power MOSFETs and IGBTs which require the application of a positive gate voltage signal in order to turn the device ON, the

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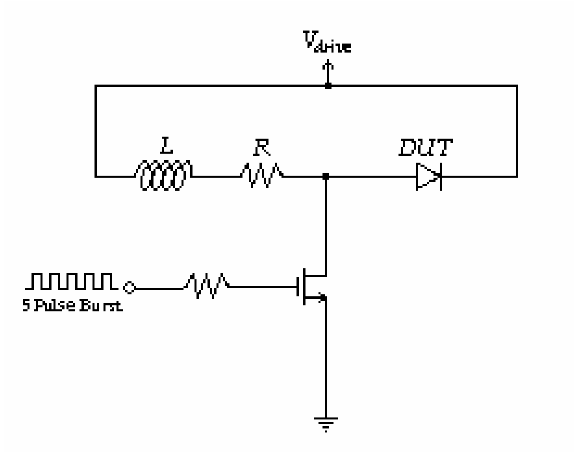

Fig. 1. Circuit diagram for the high-speed diode reverse recovery test system.

static induction transistors presented here are normally-ON devices, meaning they require the application of a negative gate voltage signal in order to turn the device OFF [5]. In the SIT structure, the gate voltage controls the current flow through the means of depletion regions that extend from the gate junctions into the n-type channel, extending deeper as an increase in the magnitude of the negative gate-to-source voltage. When the device has zero gate voltage or a small negative gate voltage, a small depletion region forms between the p^+ / n^- interface, and the channel that forms has a width of the distance between the two depletion regions. With a positive drain-source voltage, majority carrier electrons flow from the source to the drain. With large applied voltages and currents, a resistive voltage drop occurs along the length of the channel, causing a distortion in the width of the depletion layers. If the pinch-off voltage V_p is applied to the gate and a large drain to source voltage is applied to the device, full pinch-off does not occur, and current will continue to flow. In order to guarantee full pinch-off under high V_{ds} operation, a voltage must be applied to the gate that is more negative than the rated pinch-off voltage of the device. The requirement of a negative gate voltage is essential to proper device operation and is described in the following section. The on-state curves are shown in Fig. 3.

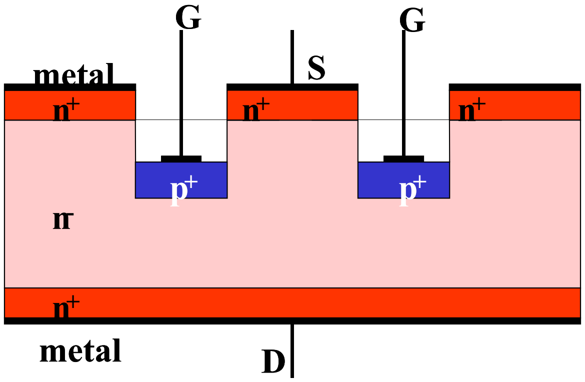

Fig. 2. Cross-section of a V-channel SIT.

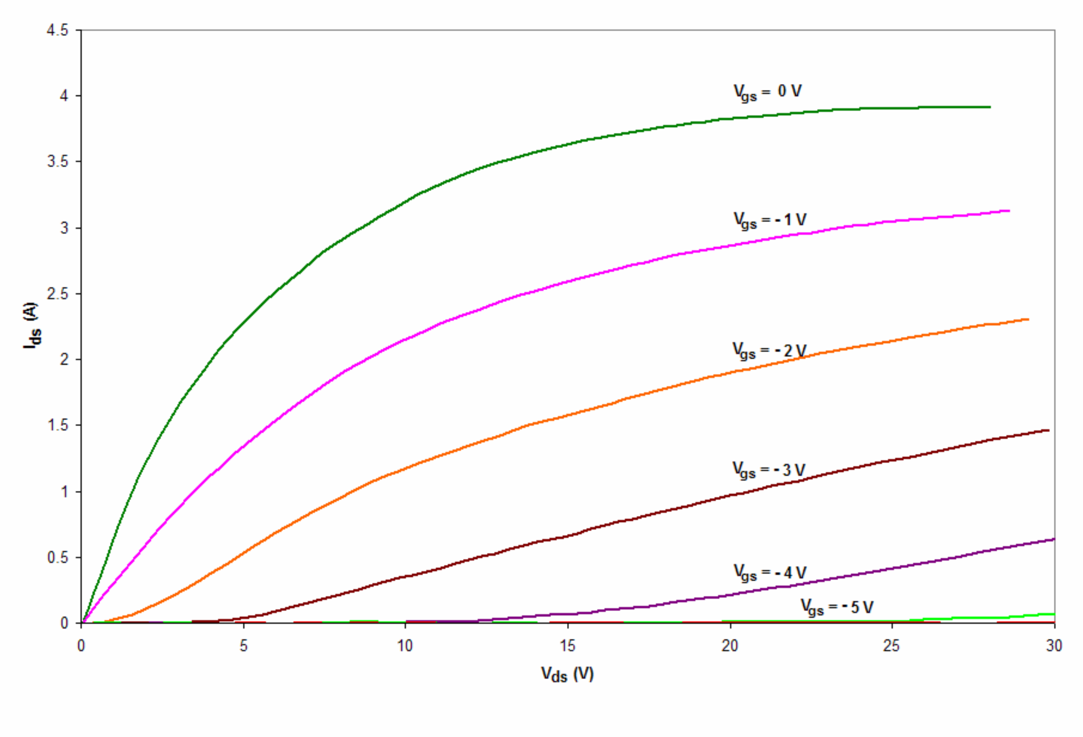

Fig. 3. On-state characteristics for the SiC Static Induction Transistor (SIT).

Due to the SIT device structure described above, it is commonly used in low voltage, high frequency applications, where parasitic device capacitances inhibit the turn-on/turn-off times of inferior switching devices. By keeping the duty cycle low in this application, the SIT is able to operate at these higher frequencies, thus providing the needed stress in testing the SiC diodes.

A typical VDMOSFET structure is shown in Fig. 4. High parasitic capacitances can be credited for severely limiting power MOSFETs' operation to frequencies well below those of the SITs: First, a capacitance can be seen in Fig. 5 that results from overlapping areas of the gate and the source. Denoted C_{gs}, the capacitance is directly proportional to the gate-source overlap area, and thus is assumed to be constant. Secondly, and more influential to switching performance, the Miller capacitance between the gate and drain, C_{gd}, determines the gate and drain currents and the drain-to-source and gate-to-source voltages [6]. Lastly, the parasitic capacitance between the drain and source, C_{ds}, which is a combination of the gate oxide capacitance and the depletion layer capacitance beneath the gate, has negligible effect on switching characteristics [7]; in any event, the end result is that the combination of the larger parasitic capacitances of the MOSFET structure limit the device's switching time and thus makes the SIT the switching device of choice for high frequency applications.

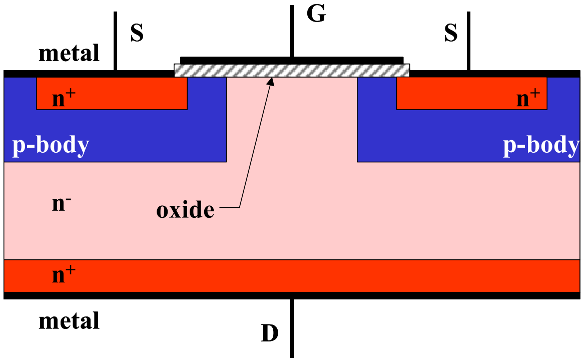

Fig. 4. Cross-section of a VDMOSFET.

SIT Gate Control

The SiC SIT gate control is essential to obtaining high voltage operation. The gate must be biased at a sufficient negative voltage in order to prevent leakage, in this case –20 V. In order to bias the gate at –20 V when the device is in the off-state, the IXYS IXDD404PI gate drive circuit was chosen for its small rise and fall times. The SIT drive circuit configuration is shown in Fig. 5. The common terminal on the gate drive circuit was connecting to the floating node between a +20 V supply and a –20 V supply. The input to the gate drive circuit was connected to the primary side of an isolation transformer, and the secondary side of the transformer was connected to the low side of the gate drive circuit.

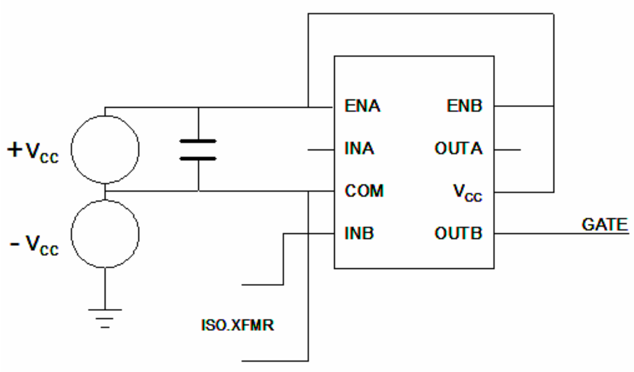

Fig. 5. Schematic for gate drive circuit.

III. CIRCUIT DESCRIPTION

Fig. 1 illustrates the developed test-bed circuit for the acquisition of SiC power diode reverse recovery characteristics. It is important to note that the circuit is very well characterized, meaning that the electrical values of all circuit components and parasitic elements within the circuit are precisely known. The circuit of Fig. 1 would normally use a power MOSFET as the control switch, but the importance of the work described here is in the replacement of that control switch with a high frequency SiC transistor; in previous work [2-4], a 6LF6 vacuum tube was substituted for the MOSFET switch to achieve low parasitic capacitance at the Device Under Test (DUT) anode as well as an extremely fast switching speed.

The implementation of such a vacuum tube control switch requires extensive knowledge of the design of the tube screen negative drive circuit, as well as requiring that the circuit be implemented between $-V_{drive}$ and 0 V. On the other hand, the three-terminal SIT only requires a function generator capable of providing a –10 V to 0 V gate-drive pulse with a variable rise/fall time.

The switch control signal used in the test-bed is a five-pulse burst triggered by a 10 Hz pulse, thus enabling the use of the SIT for tests normally outside of its range of power operation. The five-pulse burst also reduces both DUT and switch self-heating, yielding characterization of device phenomena at the intended temperature; still further, the burst eliminates the need for power supplies that provide a large value of output current, as the output filter capacitance used to minimize the ac ripple can store a sufficient amount of charge to output substantial levels of current.

The test-bed itself allows for the performance of reverse recovery tests for various values of forward diode current, V_{drive}, di_D/dt, and dv_D/dt, where the value of forward diode current is controlled by the input pulse width to the gate drive circuit, di_D/dt is controlled by varying the value of the gate resistor, and dv_D/dt is controlled by placing various capacitors across the DUT. By independently controlling these parameters, the test circuit enables testing of the new SiC technology for the full range of application conditions: Varying the value of V_{drive} emulates the application conditions for circuits with different DC buss voltages; varying the value of di_D/dt emulates the application conditions of different speed anti-parallel switching devices; varying the value of dv_D/dt emulates the application conditions of using anti-parallel switching devices of different output capacitances; and for model parameter extraction purposes, varying the value of the forward diode current at turn-off aids in the determination of the portion of diode current that is due to emitter recombination and the portion that contributes to charge storage. In addition, variation of dv_D/dt aids in the determination of the portion of the diode recovery due to charge storage and the portion due to device capacitance.

High-frequency Circuit Design

In order to properly characterize the diode under test, the test circuit must be free of parasitic and noise effects to such a degree that diode characteristics can be easily discerned. To properly observe diode reverse recovery characteristics at times on the order of 10 ns, several circuit design issues were addressed. First, the circuit layout was conceived such that all circuit components were as physically close to one another as possible, thus reducing parasitic inductance in the circuit wiring. Further reducing circuit inductance, bus bar was used for connection to V_{drive}, as a large parasitic inductance in the power supply conductors manifests itself as voltage oscillations in the diode recovery voltage. These oscillations are well over a 100 V ripple at the test voltages reported here. Third, to further reduce the voltage ripple in the power supply conductors, sufficiently-rated capacitors were placed at the power supply point of entry into the circuit between the positive and negative power supply buses. The capacitors were a mixture of capacitor types (e.g., ceramic, electrolytic, etc.) in order to filter out circuit noise. Fourth, the circuit was mounted on a ground plane, which reduces the parasitic capacitance and inductance. Lastly, the voltage and current probe leads were matched in order to provide the proper delay. On the time scale desired for testing SiC diode reverse recovery, the lead propagation delay is on the order of the device characteristics. Utilizing matched probe leads results in the voltage and current waveforms that are properly aligned in time.

IV. SIT TEST CIRCUIT RESULTS

DUT: Ultra-fast Recovery Si Diode

In Figs. 6 and 7, an initial forward current is established in the diode before the diode is switched off by applying a constant negative *di/dt* with the control switch. The switch current increases linearly until the voltage reaches the voltage supply value, V_{drive}. Fig. 6 illustrates the results of using a typical IRF820 Si MOSFET [8] in the test circuit of Fig. 1, and Fig. 7 shows the results of using the SiC SIT.

It is concluded from Figs. 6 and 7 that the SIT provides a much higher *di/dt* than does the MOSFET: 177.7 A/µs and 70.65 A/µs, respectively. As the rise time of the control signal is decreased (i.e., the gate pulse is slower to reach its final value), the *di/dt* of the DUT at turn-off increases. For the case of the Si MOSFET, decreasing the rise time (or synonymously, increasing the *di/dt* of the DUT) is restricted by the parasitic capacitances of the MOSFET structure.

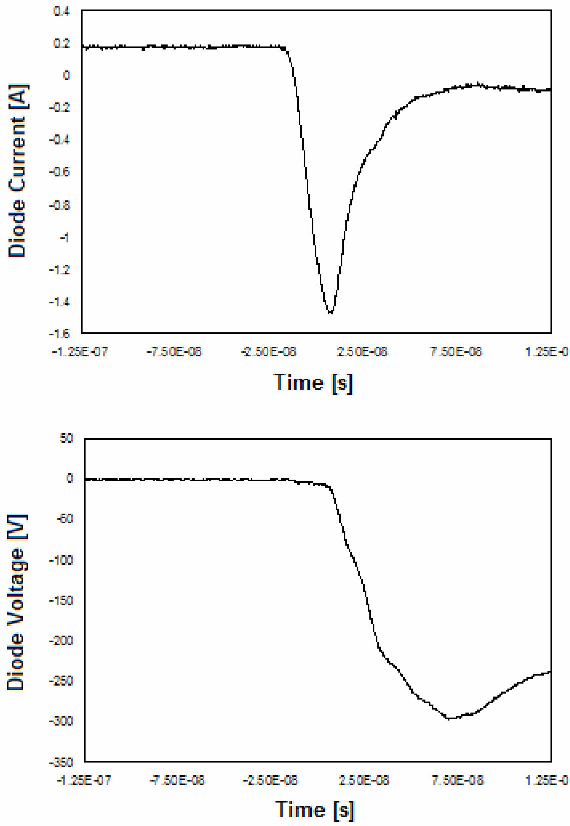

Fig. 6. Diode reverse recovery test utilizing IRF820 MOSFET.

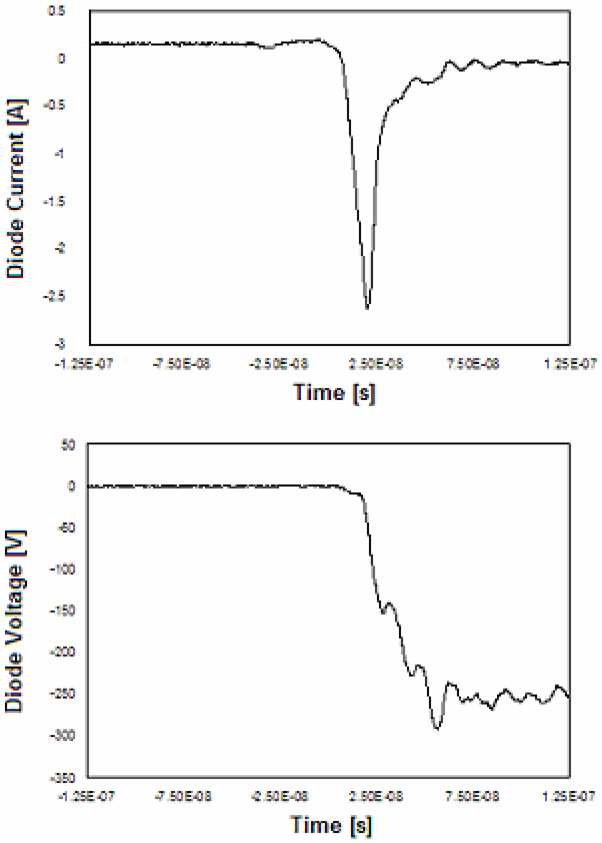

Fig. 7. Diode reverse recovery test utilizing SiC SIT.

Fig. 7 shows the results for the case of the SiC SIT. The availability to increase the *di/dt* of the DUT at DUT turn-off is improved by the reduction in parasitic capacitance of the SIT structure. The current waveform of Fig. 7 boldly demonstrates that the gate voltage can increase to its maximum value much faster than in the case of the MOSFET due to the severe reduction of the Miller capacitance offered by the SIT structure.

DUT: SiC Schottky Diode

In Figs. 8 and 9, the reverse recovery characteristics of a commercially available SiC Schottky diode [9] are shown for the test circuit using a Si MOSFET and a SiC SIT as the switching devices. The initial measured forward current is approximately 0.2 A, and the diode is switched by applying a constant negative *di/dt* with the switch. Under identical circuit conditions, the di/dt in the case of the Si MOSFET is 42.6 A/µs, and the di/dt for the SiC SIT is 64.3 A/µs.

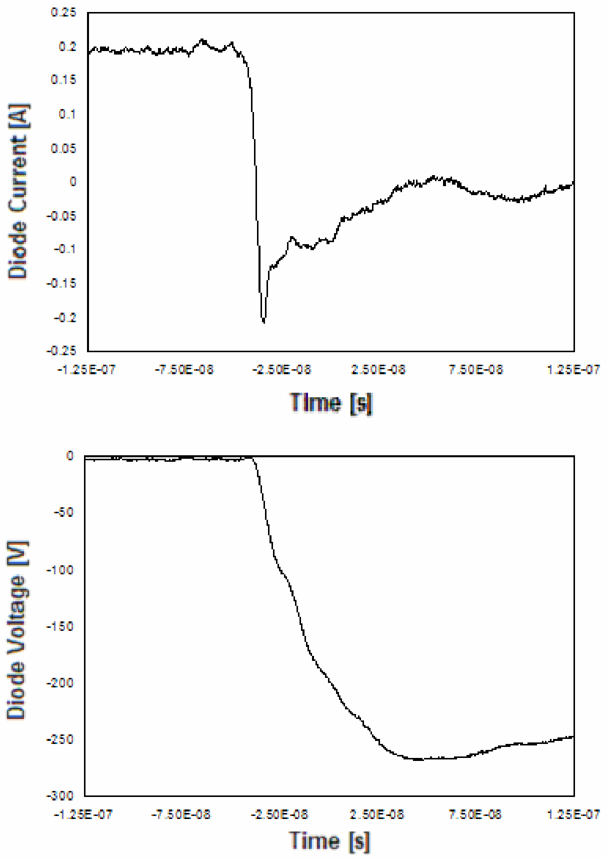

Fig. 8. SiC Schottky diode reverse recovery utilizing IRF820 MOSFET.

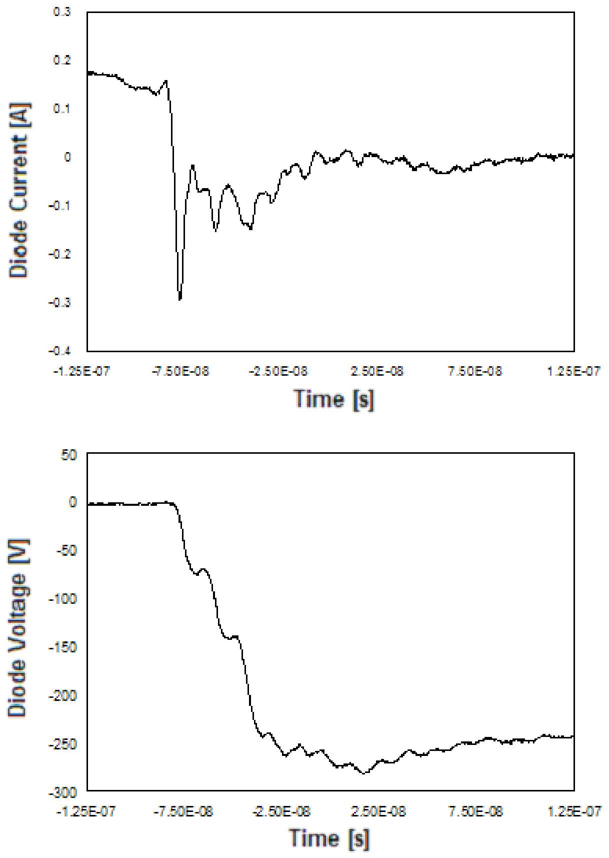

Fig. 9. SiC Schottky diode reverse recovery utilizing SiC SIT.

The SiC SIT device possesses less intrinsic device capacitance and hence operates at faster speeds than does the MOSFET. Noticeable in Fig. 8 is the MOSFET's two-phase negative voltage rise toward the voltage peak, which is due to the intrinsic gate-drain capacitances. Although a bit of ringing is shown in the waveforms, the SIT structure demonstrates a single-phase rise in the diode voltage (which is governed by the drain voltage of the SIT). This allows the test circuit to further stress the DUT as well as to free the DUT waveforms of the parasitic drain capacitance of the MOSFET, thereby forcing cleaner characterization waveforms.

V. CONCLUSION

It is shown that a SiC SIT is capable of much faster switching speeds than the traditional power MOSFET when used in the diode characterization test-bed. Due to the device structure, the SIT provides less parasitic capacitance and, ultimately, the capability to switch at much higher frequencies, while retaining the capability to adequately stress the diode under test. In addition, the SIT offers convenience as it boasts an easy to implement control system that does not require elaborate circuit design when compared to a vacuum tube.

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