

Compact Circuit Simulation Model of Silicon Carbide Static Induction and Junction Field Effect Transistors

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Abstract- The electrical characterization and model development for silicon carbide (SiC) vertical channel SIT and JFET structures are presented in this work. A compact model is developed based on the device geometry and SiC material properties. The model is validated against measured data at 25°C and 100°C for a prototype 0.03 cm² SiC SIT provided by Northrop Grumman. Validation is also done against the power JFET present in the combined MOSFET-SiC JFET cascode structure from SiCED. The model's on-state and transient characteristics are validated over this temperature range. Validation of the model shows excellent agreement with measured data. The physics-based approach implemented in this model is crucial to describing the transient behavior over a wide range of application conditions and temperature ranges.

W_{bz} Zero-bias base width (cm)
 W_{gd} Depletion width of gate-drain area (cm)

I. INTRODUCTION

Silicon carbide (SiC) power devices are expected to show superior performance compared to other semiconductor materials primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and higher temperature capability than conventional Si materials [1]. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices, the combination of $1/10^{\text{th}}$ the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed.

Of all SiC power transistors (e.g., MOSFETs, JFETs, BJTs) currently under development, SiC JFETs have perhaps the greatest near term potential for commercialization for high temperature applications. SiCED/Infineon in Europe and Semisouth Laboratories in the U.S. are two companies actively working toward this end. The availability of compact circuit simulation models for these devices will greatly aid power electronics engineers in circuit design, testing, prototyping, and product development. Presently, validated SiC power diode and MOSFET models exist that accurately describe on-state and switching conditions over a wide range of application conditions and operating temperatures [2]-[4]. The work shown here extends the previous modeling work to vertical channel junction field effect transistor (JFET) behavior. Such behavior is present in both power JFETs and static induction transistors (SITs), since their structures are very similar. In fact, the primary difference in the structures is the spacing of the gate contacts (more tightly spaced in SITs), and gate implant depths (shallower for SITs). In this paper a compact circuit simulator model has been developed for SiC JFET/SIT structures [5] as shown in Fig. 1. The model accurately describes device performance for on-state and switching characteristics for 25°C and 100°C.

NOMENCLATURE

A_g	Gate-drain overlap area (cm ²)
A_s	Gate-source overlap area (cm ²)
α	Thermionic emission factor
C_{gd}	Gate-drain depletion capacitance (F)
C_{gs}	Gate-source depletion capacitance (F)
C_{gsm}	Gate-source metallization capacitance (F)
ϵ_{SiC}	Dielectric constant of silicon carbide (F/cm)
f_{csj}	Gate-source area factor
i_o	Channel current factor (A)
I_{jfet}	JFET channel current (A)
i_{mod}	Conductivity modulated current (A)
I_{sgd}	Gate-drain junction saturation current (A)
I_{sgs}	Gate-source junction saturation current (A)
k	Boltzmann's constant (J/K)
λ	Channel modulation parameter
N_b	Base dopant density (cm ⁻³)
N_{gd}	Emission coefficient for gate-drain junction
N_{gs}	Emission coefficient for gate-source junction
P_f	Power factor coefficient
q	Fundamental electronic charge (C)
R_{mod}	Zero bias value of intrinsic region resistance (Ω)
R_d	Variable drift resistance (Ω)
R_m	Series contact resistance (Ω)
τ	Carrier lifetime (s)
V_{bi}	Built-in junction potential (V)
V_{ds}	JFET channel voltage (V)
V_{gs}	Gate-source voltage (V)
V_{gd}	Gate-drain voltage (V)
V_p	Channel pinch-off voltage (V)
V_t	Thermal voltage (V)

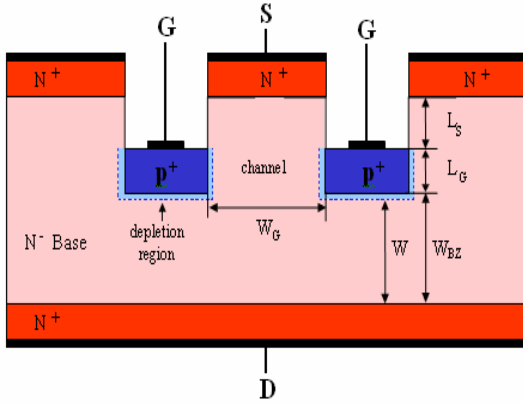


Fig. 1. Cross-sectional structure of SiC vertical JFET/SIT.

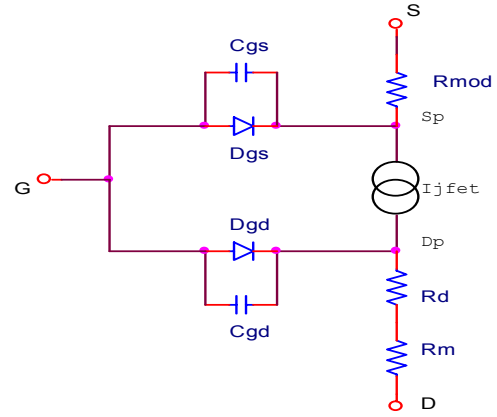


Fig. 2. Internal model topology of the SiC JFET/SIT.

TABLE I. JFET MODEL EQUATIONS

JFET/SIT channel currents	
$I_g + I_d = I_s$ <p>if $V_{ds} > 0$</p> $I_{jfet} = i_o \cdot [1 + \tanh\{P_1(V_{gs} - V_p)\}] \cdot \tanh(\alpha V_{ds}) \cdot e^{\lambda V_{ds}}$	$i_{mod} = \frac{(\mu_n + \mu_p)V_{gs}q_m}{W_{gd}^2}$ $I_{gd} = I_{sgd}(\exp(V_{gs}/n_{gs}V_i) - 1)$ $I_{gs} = I_{sgs}(\exp(V_{gd}/n_{gs}V_i) - 1)$
On-State Equations	
$W = W_{bz} - W_{gd}$ $R_d = \frac{W}{qN_b\mu_n(A_g + A_s)}$ $\mu_n = \frac{947}{1 + (\frac{N_b}{1.94 \times 10^{17}})} \left(\frac{T}{300}\right)^{-2.15}$ $q_m = \tau \cdot I_{gs}$	Transient Equations $W_{gs} = \sqrt{\frac{2\epsilon_{SiC}(V_{gs} + V_{bi})}{qN_b}}$ $C_{gs} = \frac{f_{csj}A_s\epsilon_{SiC}}{W_{gs}}$ $W_{gd} = \sqrt{\frac{2\epsilon_{SiC}(V_{gd} + V_{bi})}{qN_b}}$ $C_{gd} = \frac{A_g\epsilon_{SiC}}{W_{gd}}$

II. DESCRIPTION OF THE COMPACT JFET MODEL

Table I lists the equations that comprise the JFET/SIT model presented here. The equations listed in Table I are implemented in the MAST hardware description language and were simulated in the Saber circuit simulator [6] in order to validate the model. The model topology is shown in Fig. 2 and it clearly identifies all the elements that are modeled. Extracted model parameters at 25°C for the SIT and the JFET are shown in Table II. The model can be visualized as consisting of a source region resistance R_{mod} that is conductivity modulated by i_{mod} for positive gate voltages with respect to the source, an ideal JFET that describes the channel current I_{jfet} , a bias-dependent series base or drift region resistance R_d , and a series contact

resistance R_m . Structures like those in Fig. 1 exhibit two distinct modes of conduction, unipolar and bipolar. In the unipolar mode, the JFET acts as a majority carrier device, where electrons flow from the source to the drain. For the cross-section shown in Fig. 1, there is a depletion region at the gate-N-base layer interface from either a p-n or Schottky metal junction depending on the gate configuration. The on-state characteristics are dependent on the gate region design; specifically the channel width W_G and gate implant depth L_G [7], as illustrated in Fig. 1. Depending on the gate depth in relation to the channel width, the structure can produce FET-like “pentode” characteristics (long gate depths L_G), diode-like “triode” characteristics (short gate depths L_G), or a combination of pentode and triode characteristics referred

Therefore, the bipolar mode is not commonly employed for power switching and the majority of applications utilize the unipolar switching mode. However, the bipolar mode is modeled here with the conductivity modulated source region R_{mod} , the modulation current i_{mod} , and the minority carrier lifetime τ [3].

III. MEASURED AND SIMULATED RESULTS

This paper presents validation data for the model as compared to measured data from SiC SITs obtained from Northrop Grumman and SiC JFET structures from SiCED (cascode structures).

As seen in the on-state curves at 25°C and 100°C (Figs. 4 and 5), the model accurately replicates the four regions of operation as explained before. The model was tested and validated for different gate voltages ranging from 0 V to -4 V. When the gate voltage is negative, the device is in the unipolar mode, the prevalent mode for power switches. Moreover, the gate control circuitry is much simpler for the unipolar mode.

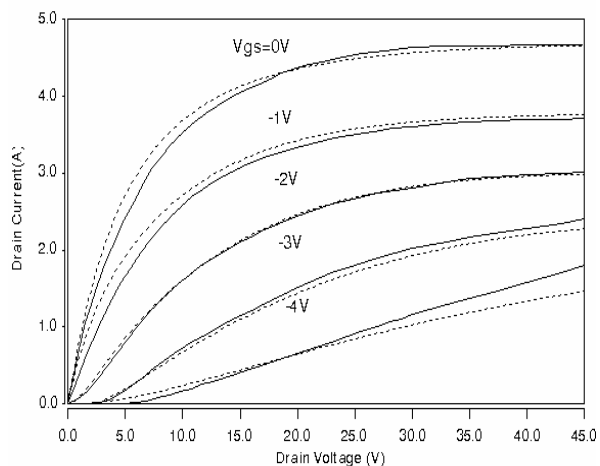


Fig. 4. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 25°C for different gate voltages.

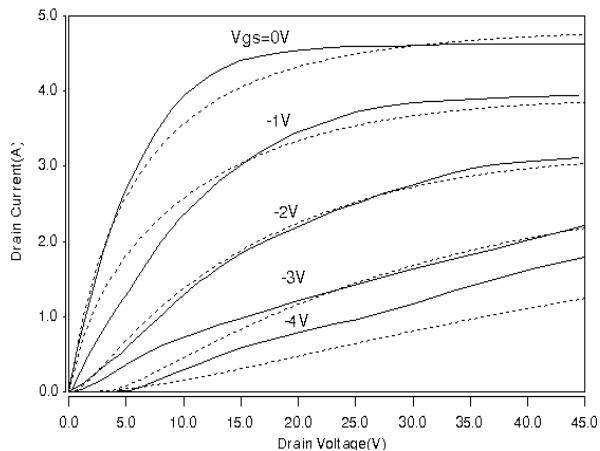


Fig. 5. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 100°C for different gate voltages.

The circuit used in the simulation for the transient response is shown in Fig. 9. It closely emulates the actual test circuit using a gate driver that switches from -16 V to 0 V for the SIT (-20 V to 0 V for the JFET), a small gate inductance, $L_g = 1$ nH, a drain series resistor, $R_L = 100\Omega$, a drain series inductance, $L_L = 1$ nH, packages capacitances, $C_{pk} = 2$ pf, and a drain supply voltage of 100 V. The gate resistance, R_g was varied (680 Ω , 1.2k Ω and 3.6k Ω for the SIT and 0 Ω and 1k Ω for the SiCED JFET) to provide different turn-on speeds for the devices. Validation results for the switching characteristics of the compact JFET/SIT model are indicated in Figs. 6 and 7 for the SIT and Fig. 8 for the JFET. In all the figures the measured data is always depicted as the solid curve while the model is indicated as a dashed curve. Fig. 6 shows the drain voltage V_{ds} , drain current I_{ds} , gate voltage V_{gs} , and gate current I_{gs} at 25°C. Fig. 7 shows the same waveforms for 100°C. A comparison of the two sets of waveforms shows that there is no considerable change in the switching time of the device even at a higher operating temperature. Fig. 8 shows the V_{ds} , I_{ds} , and V_{gs} turn-on waveforms at 25°C for the SiCED JFET.

The unipolar switching characteristics of the device can be described by the capacitances listed in Table I. For the case of the turn-on waveforms in Figs. 6 and 7, the gate voltage waveform is described by a two-phase capacitive response. During the initial rise of the gate voltage, the constant C_{gsm} and small junction capacitance C_{gsj} are charged yielding the initial slope in V_{gs} . The effect of C_{gsm} and C_{gsj} charging are also seen in the I_{gs} curves and have consequently been modeled.

Once the gate-source capacitance is charged, V_{gs} rises according to the larger gate-drain depletion capacitance C_{gdj} . The gate-drain capacitance C_{gdj} is charged until the threshold voltage V_t ($V_t = V_p - V_{bi}$) is reached, at which point the drain current flows as C_{gdj} continues charging. The higher the gate resistance, the more time it takes to charge the capacitances and therefore, the switching response gets slower as the gate resistance increases. As observed in the transient modeling results, the switching time is on the order of 0.6 μ s (for 680 Ω) and the various depletion capacitances described in the model are able to accurately predict the switching characteristics of the SiC SIT.

The transient waveforms for the JFET seen in Fig. 8 have been modeled with the same equations that were used for the SIT. But, it can be clearly seen that there is a considerable delay for I_{ds} to switch from 0 A to 1 A. This is attributed to the parasitic capacitance in the cascode structure due to the presence of the MOSFET. The device physics of the cascode structure is currently under study at the University of Arkansas and it's modeling is also under progress.

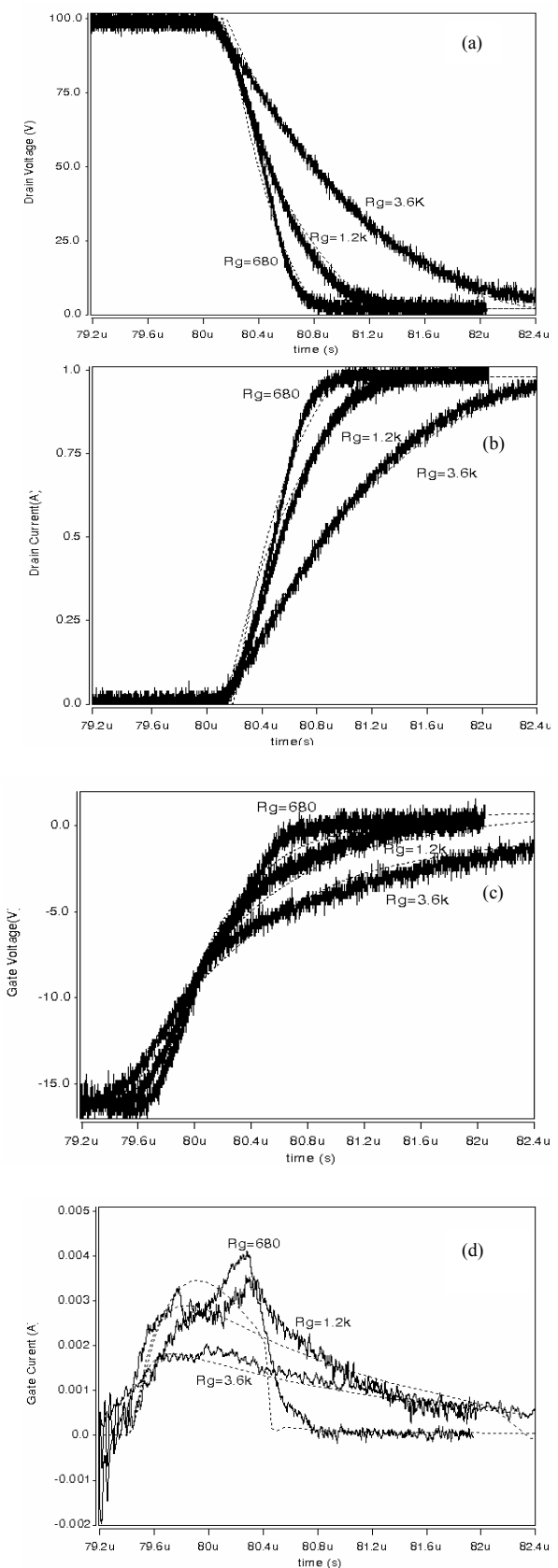


Fig. 6. Silicon carbide SIT simulated (dashed) and measured (solid) turn-on waveforms at 25°C; a) drain voltage, b) drain current, c) gate voltage and d) gate current for different gate resistances.

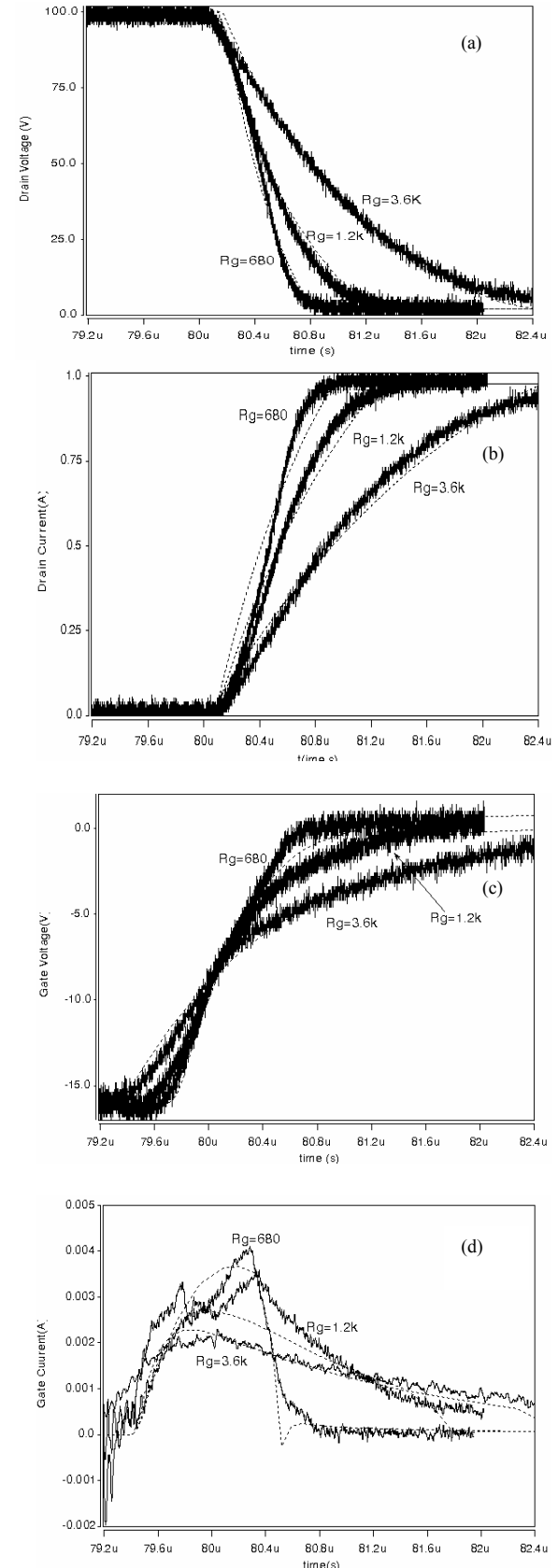


Fig. 7. Silicon carbide SIT simulated (dashed) and measured (solid) turn-on waveforms at 100°C; a) drain voltage, b) drain current, c) gate voltage and d) gate current for different gate resistances.

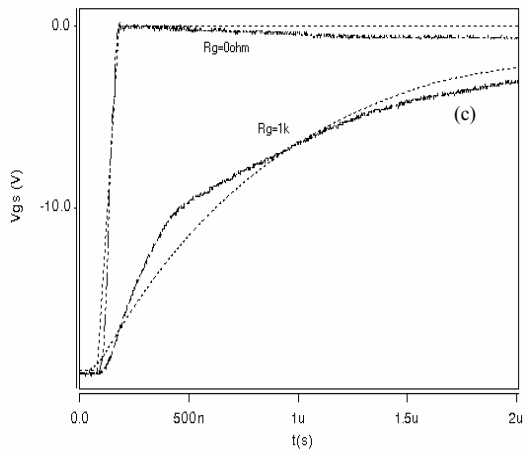
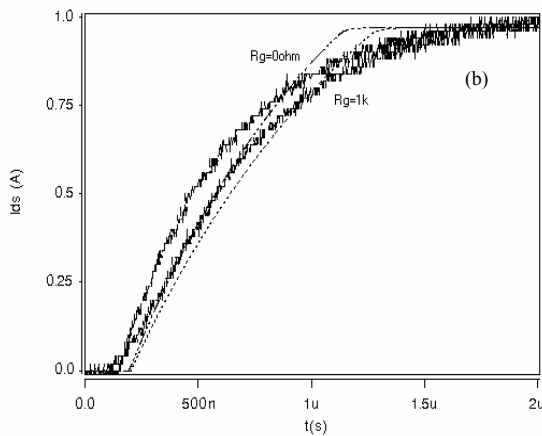
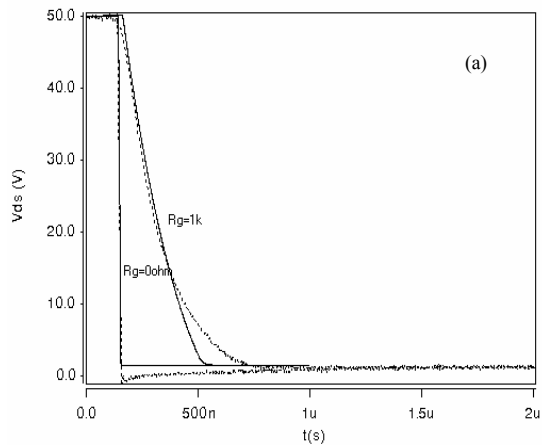


Fig. 8. Silicon carbide JFET simulated (dashed) and measured (solid) turn-on waveforms at 25°C; a) drain voltage, b) drain current, and c) gate voltage.

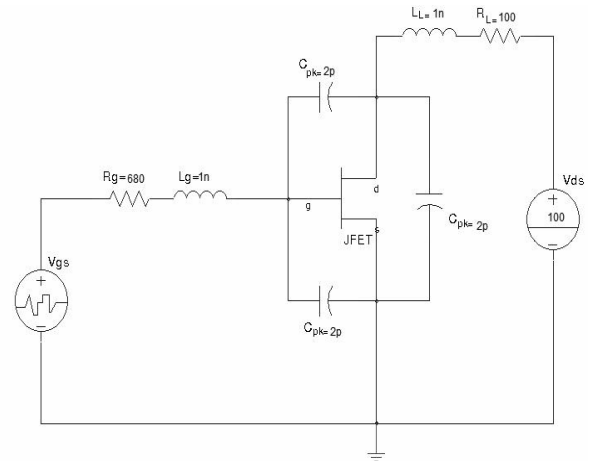


Fig 9: Simulation test bench for the transient analysis of the SiC SIT/JFET

IV. CONCLUSION

A compact SiC power JFET/SIT model has been developed and demonstrated for use in circuit simulators. The model is a combination of empirical relations for on-state behavior, and temperature and material based device physics equations that accurately replicate the transient behavior of the device. The model was shown here to accurately describe the on-state and transient characteristics at 25°C and 100°C for the SIT. The SiC JFET has also been successfully modeled as seen in the transient curves for the same. Future work will involve characterization of the model against JFET devices from SemiSouth Laboratories.

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