VHDL-AMS Modeling of Silicon Carbide Power Semiconductor Devices

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Abstract- **VHDL-AMS is gaining ground as the standard modeling language for devices and systems. A new modeling tool, Paragon[1], is presented in this work that helps the user to create models with only the topology and the characteristic equations. Paragon then generates the model in various HDLs such as VHDL-AMS, MAST and Verilog-A. As an example, a silicon carbide vertical JFET/SIT is modeled using Paragon. SiC JFETs are power switches that have a variety of applications in the industry. A compact model is developed in VHDL-AMS based on the device geometry and SiC material properties. The on-state model has been tested in Mentor Graphics' Systemvision VHDL-AMS simulator and it clearly replicates the behavior seen in experimental characterization as the validation results show.**

I. INTRODUCTION

Power electronic designers have been constrained in the past due to the limited availability of reliable, compact power device models in commercial simulators. Semiconductor device modeling is a time-consuming and error-prone task. Historically, adding models to simulators was so difficult that only simulator specialists dared to attempt the task. With the advent of Hardware Description Languages (HDLs), this task became easier because the amount of simulator/algorithm/data structure-specific work was mostly eliminated. Now the model developer could focus more strictly on the characteristics of the device being modeled. This has been the situation for over a decade and yet there is still room for improvement. HDL modeling is still programming, thus tedious, error-prone, and difficult to debug. Modeling tools that raise the level of model input, debug, and reuse to a conceptual level above the HDL implementation are therefore desirable.

HDL-based modeling involves (i) Understanding the device physics and constructing the topology of the device (ii) Formulating the model in the HDL and (iii) Testing and validating the model against the actual device measurements. All three steps involve considerable effort, which contributes to the overall model development time. A new model development tool, Paragon [1-2], is described in this paper. Paragon is a language independent, mixed-signal behavioral modeling environment. Paragon greatly aids the modeler by generating models in multiple HDLs such as: VHDL-AMS [3], MAST [4], Verilog–A and C++ code for Spice-like simulators. It reduces model development time since all model information is entered graphically along with the corresponding characteristic equations. Further, it promotes reuse of the model and eases the burden of supporting and modifying the model.

Silicon Carbide devices are gaining attention from the power electronics community due to their high electric field breakdown and excellent thermal conductivity [5]. This allows SiC devices to be deployed in high power and high temperature applications. Cree Inc. has commercially released SiC Schottky diodes. It appears that power JFETs and MOSFETs will soon be available. This makes it imperative that the models for these SiC devices are available when they are commercially released. Validated SiC power diode and MOSFET models have already been developed [6-8] and this work extends it to the vertical JFET/Static Induction Transistors (SIT). JFETs are excellent power switches due to their fast switching times and high temperature capabilities. Therefore, they have many potential applications in automobiles, aeronautics, energy conversion etc. Moreover, due to the radiation-hard nature of SiC, these devices are also of interest to the aerospace industry.

In this paper, a compact circuit simulator model for a SiC power JFET is described. The model was implemented in Paragon, generated in VHDL-AMS and accurately describes the on-state device performance. The structure of the JFET is shown in Fig. 1. VHDL-AMS is currently gaining ground as the industry standard (IEEE standard 1076.1) modeling language and therefore this effort focuses on developing power device models in this standard.

II. DESCRIPTION OF THE COMPACT JFET MODEL

For this modeling effort, a Northrop Grumman prototype SiC SIT has been used. SITs and vertical JFETs have very similar structure and they differ only by the relative spacing of the gates (Fig. 1). Depending on the gate depth in relation to the channel width, the structure can produce FET-like "pentode" characteristics (long gate depths L_G), diode-like "triode" characteristics (short gate depths L_G), or a combination of pentode and triode characteristics referred to as "mixed-mode" characteristics (intermediate gate depths L_G). For devices optimized for power switching applications, the device typically exhibits mixed-mode characteristics [9]. SITs have four distinct

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regions of operation – (i) Ohmic (ii) Thermionic (iii) Space charge limited current (SCLC) (iv) SCLC with velocity saturation. For higher gate voltages, ohmic behavior is observed, whereas for lower gate bias, thermionic effect dominates. The model can be visualized as consisting of a source region resistance R_{mod} that is conductivity modulated by i_{mod} for positive gate voltages with respect to the source, an ideal JFET that describes the channel current I_{jfet}, a bias-dependent series base or drift region resistance R_d, and a series contact resistance R_m. The various mathematical relations used in the model and the extracted parameters at 25°C are given in Tables 1 and 2.

The model presented in this paper utilizes a semi-empirical approach for the on-state modeling [10] – [11]. The equation for the on-state modeling uses a hyperbolic tangent function that contains empirical parameters. The channel current factor i_o can be varied to adjust the absolute current level in the device. The model also has empirically determined polynomial relations c and d, which are used to adjust the slope of the resulting current. The thermionic emission factor α is an empirical relation that determines the amount of thermionic emission current in the model, and also has a temperature dependency that allows the user to model the device for a range of temperatures. These variables (α, c and d) are functions of V_{gs}.

The model developed here in VHDL-AMS clearly replicates all the four regions accurately and it has been successfully validated with actual measured data from a device. The on-state model uses a single current equation, which avoids some common simulator convergence problems and thus reduces the computation time. The model has been optimized for unipolar switching, in which the gate voltage remains negative and only electrons conduct and therefore there are no storage effects. In the bipolar mode, holes are injected from the gate and there is higher conduction. This results in a lower switching speed and more complex gate drive requirements. Therefore, this is not a preferred mode for power switching applications.

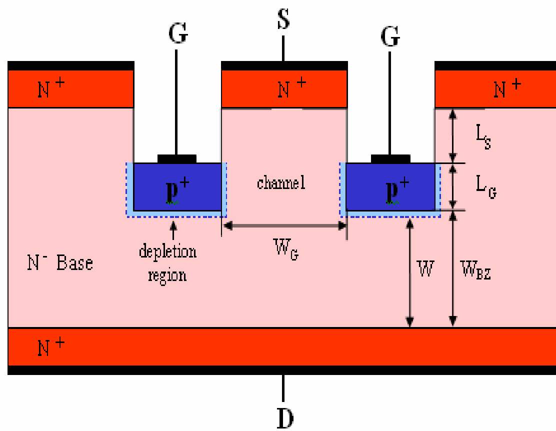

Fig. 1. Cross-sectional structure of SiC vertical JFET/SIT.

III. MODELING METHODOLOGY IN PARAGON

The terminals and parameters are first entered in the Model Interface Editor (MIE) as seen in Fig. 2. The MIE allows the user to specify the model name, connection points, parameters (user defined), regions of validity of the parameters, and default values of the parameters of a model.

This will automatically generate pins for the model from which a symbol can be created using the symbol editor. Geometrical shapes can be easily constructed in the symbol editor, which is automatically linked to the model. The topology of the model can be captured using the Topology Editor (Fig. 3).

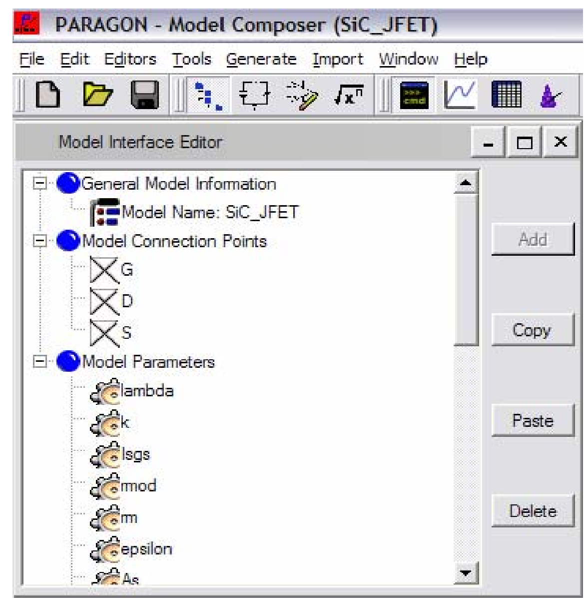

Fig. 2. Screenshot of the Model Interface Editor.

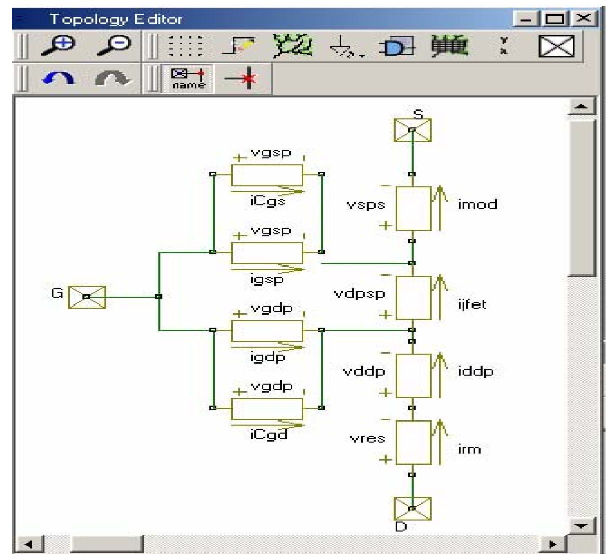

Fig. 3. Screenshot of Topology Editor.

TABLE I. JFET MODEL EQUATIONS

JFET/SIT channel currents

$I_g + I_d = I_s$

if $V_{ds} >= 0$

$I_{jfet} = i_o \cdot [1 + \tanh\{P_1(V_{gs} - V_p)\}] \cdot \tanh(\alpha V_{ds}) \cdot e^{\lambda V ds}$

$P_1 = 1 + 0.05(V_{gs})$

On-State Equations

$W = W_{bz} - W_{gd}$

$$R_d = \frac{W}{qN_b \mu_n (A_g + A_s)}$$

$$\mu_n = \frac{947}{1 + (\frac{N_b}{1.94x10^{17}})} (\frac{T}{300})^{-2.15}$$

$q_m = \tau \cdot I_{gs}$

$$i_{mod} = \frac{(\mu_n + \mu_p) V_{gs} q_m}{W_{gd}^{\ 2}}$$

$I_{gd} = I_{sgd}(\exp(V_{gs}/ngs \cdot V_t) - 1)$

$I_{gs} = I_{sgs}(\exp(V_{gd}/ngs \cdot V_t) - 1)$

Transient Equations

$$W_{gs} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gs} + V_{bi})}{qN_b}}$$

$$C_{gs} = \frac{f_{csj} A_s \varepsilon_{SiC}}{W_{gs}}$$

$$W_{gd} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gd} + V_{bi})}{qN_b}}$$

$$C_{gd} = \frac{A_g \varepsilon_{SiC}}{W_{gd}}$$

A model can be represented by a set of branches where each branch describes a particular behavior of the model. Each branch is associated with a 'through' and 'across' variable which are the system variables. A branch also has characteristic equations that relate the through and across variables. For an electrical system, voltages are the across variables and currents are the through variables, following energy conservation laws such as KCL and KVL. The Equation Editor (Fig. 4) can used to define differential-algebraic equations, implicit relationships, conditional relations, and assignments that are used to define mathematical or functional behavior.

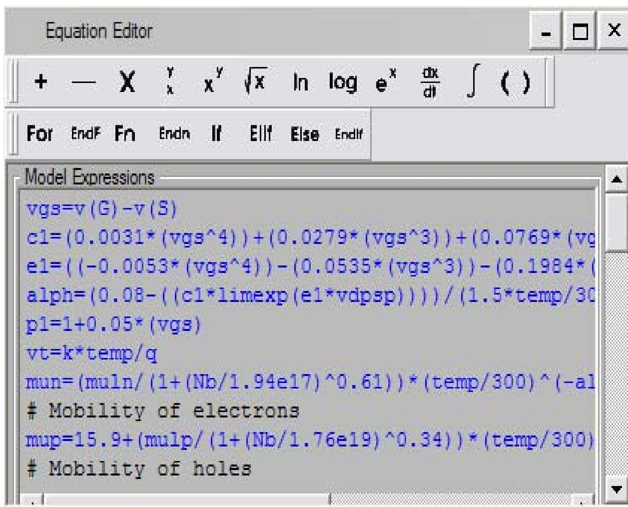

Fig. 4. Screenshot of the Equation Editor.

For example, in the Topology Editor between the drain terminal *d* and the internal node *dp*, there is a branch that has *vddp* as the across variable and *iddp* as the through variable. *iddp* is defined as *vddp*/R_s, where R_s is the contact resistance, a model parameter.

After entering the required information of the JFET model in the Paragon interface, the VHDL-AMS code is generated from the 'Generate button' in the tools menu. For brevity, the salient parts of the generated VHDL-AMS code are given below:

```
library IEEE; -- Library declarations
use IEEE.math_real.all;
use IEEE.electrical_systems.all;

------ Model Interface and Parameters Declaration ------
entity SiC_JFET is
generic ( vbi:real:=2.8;
wbz:real:=10.0e-4;
Isgd:real:=1.0e-30;
As:real:=0.01;
………
………-- All the parameters are declared here

port (terminal S: electrical; terminal D: electrical; terminal
G: electrical);
end entity SiC_JFET;

architecture behavior of SiC_JFET is
terminal dp: electrical; -- internal nodes
terminal sp: electrical;
```

```
----------- Branch Variable Declarations ---------
quantity vgs across G to S;
quantity igdp through G to dp;
quantity vgdp across G to dp;
quantity ijfet through dp to sp;
quantity vdpsp across dp to sp;
....
-------------- Simultaneous Equations -------------
....
if vdpsp'above (0.0) use
ijfet==(((io*(1.0+(tanh((p1)*(vgsp-
vp)))))*(tanh(alph*vdpsp)))*(limit_exp(lambda*vdpsp)));
else
ijfet==0.0;
end use;
break on vdpsp'above (0.0);
iddp==(vddp/(rm));
.....
end architecture behavior;
-----------------------------------------------------------------
```

TABLE II. MODEL PARAMETERS AT 25°C

Parameter	Value
Vp	6 V
Wbz	100.0×10^{-4}cm
As	0.015 cm^2
Ag	0.015 cm^2
fcsj	0.2
Nb	2.0×10^{15} cm^{-3}
Isgs	1.0×10^{-35}A
Ngs	2
Isgd	1.0×10^{-35}A
Ngd	2
io	4.2×10^{7}
Vbi	2.8 V
Rm	0.1 Ω
Rmod	0.5 Ω
Tau	0 ns
Lambda	5.0×10^{-4}

The VHDL-AMS model was then tested in Mentor Graphics' Systemvision simulator and the on-state characteristics at 25°C and 100°C respectively.

The DC curves show the four regions of operation that manifest in the SIT. In Fig. 5, for the V_{gs}=0 V and -1 V curves, I_{ds} is clearly ohmic until about 5V and then the space charge limited current dominates. For lower V_{gs} values, the thermionic effect (similar to diode action) can be seen before the SCLC. At high values of V_{ds}, velocity saturation occurs and the DC curves at V_{gs} = 0 V and -1 V are therefore seen to saturate.

As seen in the on-state curves at 25°C and 100°C (Figs. 5 and 6), the model accurately replicates the four regions of operation as explained before. The model was tested and validated for different gate voltages ranging from 0 V to -4 V. When the gate voltage is negative, the device is in the unipolar mode, the prevalent mode for power switches.

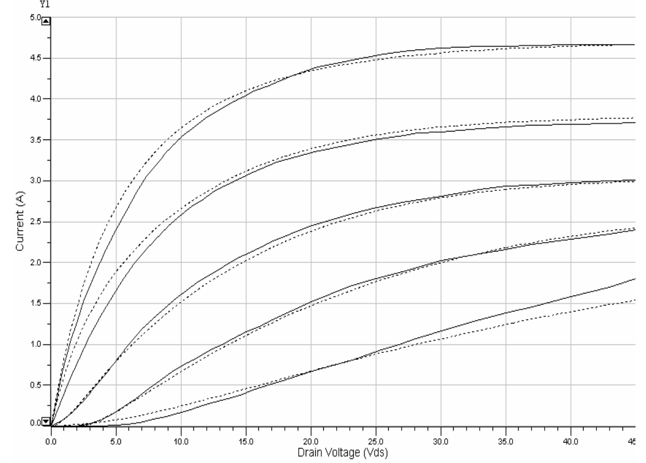

Fig. 5. Silicon carbide SIT simulated (dashed) and measured (solid) on-state waveforms at 25°C for different gate voltages.

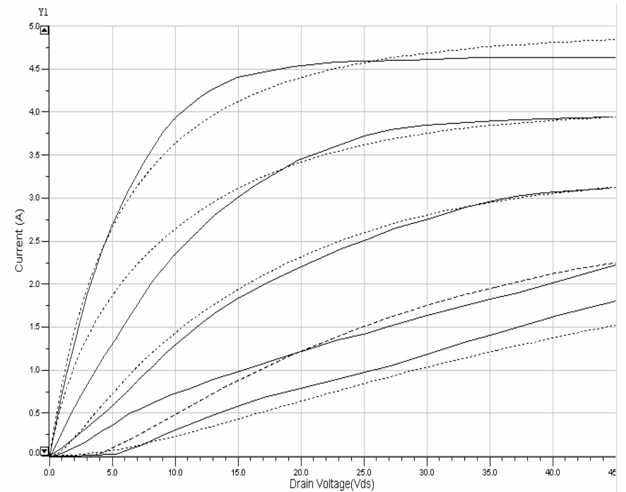

Fig .6. Silicon carbide SIT simulated (dashed) and measured (solid) on-state. waveforms at 100°C for different gate voltages.

IV. EMERGING TECHNOLOGY

Spice emerged in the 1970's and established itself as a standard simulator in the field of modeling and simulation. Before the advent of HDLs, Spice and its derivatives were the only choice for circuit simulation. Implementing a new model and making it available in Spice for simulations was an arduous task. It requires a deep understanding of the underlying simulator concepts and algorithms. The birth of HDLs in the 1980's made it easy to describe a model in a more intuitive programming style. This segregated all the model information from the simulator intricacies and eased the task of developing new models. Though HDLs are not a substitute for Spice, their language definitions contain many more primitives that can simplify the process of creating

behavioral models. A behavioral model can be created using HDLs just as accurately as in Spice or even better, especially when characterizing the behavior of actual devices. The scope of these languages extends to mixed technology systems as well.

As Device modelers are not inclined to programming, tools were developed in the 90's [1,12] which aided model prototyping and represented a model graphically, making it more intuitive. The learning curve for these tools is not steep and the greatest advantage of them is providing readable, error free and standardized code which reduces unnecessary iterations. The support for these models is available in HDL-specific simulators such as Saber (MAST) and ADMS (VHDL-AMS) which are not considered low-cost simulators. To utilize the real power of both HDLs and widely acceptable Spice simulators, Model Compilers [13] are gaining attention in recent times. The main objective of these Model Compilers is to convert a high level HDL to a low-level C code, which can be used in a Spice simulator.

All the symbolic derivation, matrix element stamping and optimization are performed in the internal architecture of Compilers. The code generation module analyses all the model equations at a language independent level by an Abstract Syntax Tree (AST), which is an internal data representation of all the governing equations. The AST represents the inter-relationships among the variables and constants in the model equations and expressions. Analysis of the AST results in the determination of the functional dependency and time dependency characteristics of the variables of the model. This enables the generation of efficient code. So the combination of model prototyping tools and model compilers bring the real power of flexibility of HDLs and making those models available in low-cost and widely used Spice simulators, thereby making them more attractive for power electronic designers.

V. CONCLUSION

A compact SiC power JFET/SIT model was developed in the Paragon modeling tool and subsequently generated in the IEEE standard VHDL-AMS HDL for validation. Since it is available in VHDL-AMS, it can be used in any number of commercial simulators. Semiconductor Device models like EKV 2.6 MOSFET simulated in Spice like simulator was implemented in 6 days in Paragon against hand-written code which was completed in 60 days. The BSIM3 MOSFET model was implemented in Paragon in 3 weeks compared to 6 months when implemented manually. The model in this paper is a combination of empirical relations for on-state behavior, and temperature and material based device physics equations that accurately replicate the transient behavior of the device. The model was shown here to accurately describe the on-state characteristics at 25°C and 100°C.

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