High Temperature Characterization and Compact Modeling of Silicon Carbide Static Induction and Junction Field Effect Transistors

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Abstract- **The electrical characterization and model development for silicon carbide (SiC) vertical channel SIT and JFET structures are presented in this work. A compact model is developed based on the device geometry and SiC material properties. The model is validated against measured data at 25°C and 100°C for a prototype 0.03 cm^2 SiC SIT provided by Northrop Grumman. Validation is also done against the power JFET present in the combined MOSFET-SiC JFET cascode structure from SiCED. The model's on-state and transient characteristics are validated over this temperature range. Validation of the model shows excellent agreement with measured data. The physics-based approach implemented in this model is crucial to describing the transient behavior over a wide range of application conditions and temperature ranges. SiCED VJFETs are also characterized at temperatures of up to 450°C to study the electrical behavior of SiC devices at such elevated temperatures.**

NOMENCLATURE

A_g	Gate-drain overlap area (cm^2)
A_s	Gate-source overlap area (cm^2)
α	Thermionic emission factor
C_{gd}	Gate-drain depletion capacitance (F)
C_{gs}	Gate-source depletion capacitance (F)
C_{gsm}	Gate-source metallization capacitance (F)
ε_{SiC}	Dielectric constant of silicon carbide (F/cm)
f_{csj}	Gate-source area factor
i_o	Channel current factor (A)
I_{jfet}	JFET channel current (A)
i_{mod}	Conductivity modulated current (A)
I_{sgd}	Gate-drain junction saturation current (A)
I_{sgs}	Gate-source junction saturation current (A)
k	Boltzmann's constant (J/K)
λ	Channel modulation parameter
N_b	Base dopant density (cm^{-3})
N_{gd}	Emission coefficient for gate-drain junction
N_{gs}	Emission coefficient for gate-source junction
P_1	Power factor coefficient
q	Fundamental electronic charge (C)
R_{mod}	Zero bias value of intrinsic region resistance (Ω)
R_d	Variable drift resistance (Ω)
R_m	Series contact resistance (Ω)
τ	Carrier lifetime (s)
V_{bi}	Built-in junction potential (V)
V_{ds}	JFET channel voltage (V)
V_{gs}	Gate-source voltage (V)
V_{gd}	Gate-drain voltage (V)
V_p	Channel pinch-off voltage (V)
V_t	Thermal voltage (V)
W_{bz}	Zero-bias base width (cm)
W_{gd}	Depletion width of gate-drain area (cm)

I. INTRODUCTION

Silicon Carbide (SiC) has many inherent properties that make it an ideal semiconductor material useful for high-temperature, high-power and radiation-hard applications [1]. Table I compares the salient features of SiC with other semiconductor materials. As seen in Table I, the bandgap of 4H-SiC is nearly 3 times that of Si. This translates to a very high breakdown field (nearly 10 times that of Si) suitable for power applications. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices, the combination of 1/10th the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed.

The saturated electron velocity of SiC which determines the maximum current density of the device is also twice that of Si. Another important property is the thermal conductivity of SiC, which is more than three times that of Si. Furthermore, the large bandgap obviates the need to have bulky and expensive cooling systems for the devices. This in turn translates into high cost savings in mass critical applications such as fighter planes and space shuttles.

Of all SiC power transistors (e.g., MOSFETs, JFETs, BJTs) currently under development, SiC JFETs have perhaps the greatest near term potential for commercialization for high temperature applications. SiCED/Infineon in Europe and Semisouth Laboratories in the U.S. are two companies actively working toward this end. The availability of compact circuit simulation models for these devices will greatly aid power electronics engineers in circuit design, testing, prototyping, and product development. Presently, validated SiC power diode and MOSFET models exist that accurately describe on-state and switching conditions over a wide range of application conditions and operating temperatures [2]-[4]. The work shown here extends the previous modeling work to vertical channel junction field effect transistor (JFET) behavior. Such behavior is present in both power JFETs and static induction transistors (SITs), since their structures are very similar. In fact, the primary difference in the structures is the spacing of the gate contacts (more tightly spaced in SITs), and gate implant depths (shallower for SITs). In this paper a compact circuit simulator model has been developed for SiC

Table I. Comparison of key characteristics of SiC with other semiconductor materials

Property	Si	GaAs	4H-SiC	6H-SiC
Bandgap (eV)	1.1	1.42	3.2	3.0
Relative dielectric constant	11.9	13.1	9.7	9.7
Breakdown field (MV/cm)	0.25	0.3	2.2	~2.3
Thermal conductivity (W /cm K)	1.5	0.5	4.8	3-5
Electron mobility (cm^2/V-s) @$N_d = 10^{16}/cm^3$	1200	6500	800	60
Hole mobility (cm^2/V-s) @$N_d = 10^{16}/cm^3$	420	320	115	90
Saturated electron velocity ($x10^7$cm/s)	1	1.2	2	2

JFET/SIT structures [5] as shown in Fig. 1. The model accurately describes device performance for on-state and switching characteristics for 25°C and 100°C. In addition to developing compact models, high temperature characterization of JFETs were also done at the University of Arkansas to demonstrate the feasibility of SiC JFETs for extreme environments.

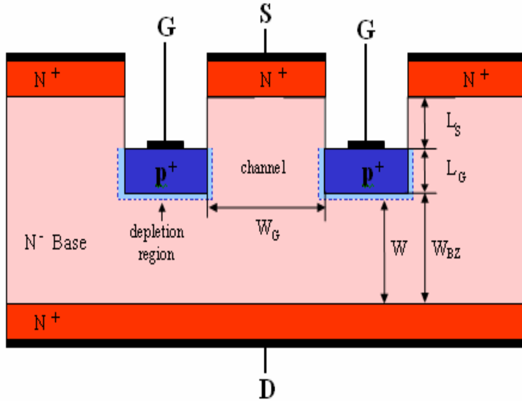

Fig. 1. Cross-sectional structure of SiC vertical JFET/SIT.

II. DESCRIPTION OF THE COMPACT JFET MODEL

Table II lists the equations that comprise the JFET/SIT model presented here. The equations listed in Table II are implemented in the MAST hardware description language and were simulated in the Saber circuit simulator [6] in order to validate the model. The model topology is shown in Fig. 2 and it clearly identifies all the elements that are modeled. Extracted model parameters at 25°C for the SIT and the JFET are shown in Table III. The model can be visualized as consisting of a source region resistance R_{mod} that is conductivity modulated by i_{mod} for positive gate voltages with respect to the source, an ideal JFET that describes the channel current I_{jfet}, a bias-dependent series base or drift region resistance R_d, and a series contact resistance R_m.

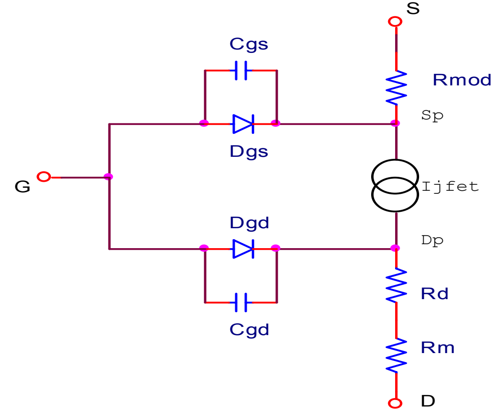

Fig. 2. Internal model topology of the SiC JFET/SIT.

Structures like those in Fig. 1 exhibit two distinct modes of conduction, unipolar and bipolar. In the unipolar mode, the JFET acts as a majority carrier device, where electrons flow from the source to the drain. For the cross-section shown in Fig. 1, there is a depletion region at the gate-N- base layer interface from either a p-n or Schottky metal junction depending on the gate configuration. The on-state characteristics are dependent on the gate region design; specifically the channel width W_G and gate implant depth L_G [7], as illustrated in Fig. 1. Depending on the gate depth in relation to the channel width, the structure can produce FET-like "pentode" characteristics (long gate depths L_G), diode-like "triode" characteristics (short gate depths L_G), or a combination of pentode and triode characteristics referred to as "mixed-mode" characteristics (intermediate gate depths L_G). For devices optimized for power switching applications, the device typically exhibits mixed-mode characteristics [7]. For sufficiently negative gate voltages when the channel is "pinched off" due to the intersecting depletion regions, the mixed-mode characteristics may be described by the thermionic emission theory when the device operates in triode region at low currents. Whether this phenomenon manifests itself is a function of the gate spacing or channel width W_G. As V_{ds} is increased, these structures produce the typical linear and saturation regions.

The mixed mode characteristics of the SIT structure can be broken into four regions of operation – (i) ohmic (ii) thermionic (iii) space charge limited current (SCLC) and (iv) SCLC with velocity saturation (V_{sat}) [8] depending on the gate design. Ohmic behavior is seen for less negative values of V_{gs} and thermionic effects are more dominant for more negative gate biases.

The cascode structure shown in Fig. 3 [9]-[10] has a power JFET which exhibits the pentode-like characteristics. The pin arrangement in the cascode package is such that the JFET can be tested independently. The drain current I_{ds} in such devices consists of only a linear and a saturation region. The model presented in this paper utilizes a semi-

Table II. SIT/JFET model equations

JFET/SIT channel currents

$$I_g + I_d = I_s$$

$$if\ V_{ds}>=0$$

$$I_{jfet}= i_o\cdot[1+tanh\{P_1(V_{gs}-V_p)\}]\cdot tanh(\alpha V_{ds})\cdot e^{\lambda Vds}$$

On-State Equations

$$W = W_{bz} - W_{gd}$$

$$R_d = \frac{W}{qN_b\mu_n(A_g + A_s)}$$

$$\mu_n = \frac{947}{(1+(\frac{N_b}{1.94x10^{17}}))^{0.61}}(\frac{T}{300})^{-2.15}$$

$$q_m = \tau\cdot I_{gs}$$

$$i_{mod} = \frac{(\mu_n + \mu_p)V_{gs}q_m}{W_{gd}^{\ 2}}$$

$$I_{gd} = I_{sgd}(exp(V_{gs}/ngs\cdot V_t)-1)$$

$$I_{gs} = I_{sgs}(exp(V_{gd}/ngs\cdot V_t)-1)$$

Transient Equations

$$W_{gs} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gs}+V_{bi})}{qN_b}}$$

$$C_{gs} = \frac{f_{csj}A_s\varepsilon_{SiC}}{W_{gs}}$$

$$W_{gd} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gd}+V_{bi})}{qN_b}}$$

$$C_{gd} = \frac{A_g\varepsilon_{SiC}}{W_{gd}}$$

empirical approach for the on-state modeling [11] – [12] and traditional device physics relations for the transient model. The equation for the on-state modeling uses a hyperbolic tangent function that contains empirical parameters. The channel current factor i_o can be varied to adjust the absolute current level in the device. The model also has empirically determined polynomial relations *c* and *d*, which are used to adjust the slope of the resulting current.

Table III. Model Parameters at 25°C

Parameter	SIT	JFET
Vp	6 V	1V
Wbz	100.0×10^{-4}cm	100.0×10^{-4}cm
As	0.015 cm^2	0.02 cm^2
Ag	0.015 cm^2	0.02 cm^2
fcsj	0.2	0.4
Nb	2.0×10^{15} cm^{-3}	2.0×10^{15} cm^{-3}
Isgs	1.0×10^{-35}A	1.0×10^{-35}A
Ngs	2	2
Isgd	1.0×10^{-35}A	1.0×10^{-35}A
Ngd	2	2
io	4.2×10^{7}	5.2×10^{4}
Vbi	2.8 V	2.8 V
Rm	0.1 Ω	0.5Ω
Rmod	0.5 Ω	0.5 Ω
Tau	0 ns	0 ns
Lambda	5.0×10^{-4}	3.0×10^{-2}

The thermionic emission factor α is an empirical relation that determines the amount of thermionic emission current in the model and it also has a temperature dependency that allows the user to model the device for a range of temperatures. It is observed that a single current equation is able to accurately describe all the different effects in the on-state. This provides better convergence in the simulator as piecewise defined equations are avoided.

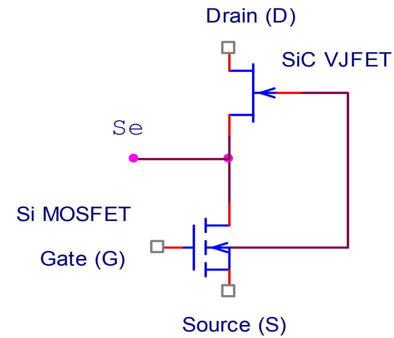

Fig. 3. SiC JFET-Si MOSFET cascode structure from SiCED

The empirical parameters c and d can be set to zero while modeling the JFET structure. In this case, α is used to adjust the linear portion of the DC characteristics and variables such as P_1 and i_o are used to adjust the saturation current level.

Fig. 5 shows the on-state response of the SIT at 25°C and Fig. 6 shows the same at 100°C. The DC curves show the four regions of operation that manifest in the SIT. In Fig. 5, for the V_{gs}=0 V and -1 V curves, I_{ds} is clearly ohmic until about 5V and then the space charge limited current dominates. For lower V_{gs} values, the thermionic effect (similar to diode action) can be seen before the SCLC. At high values of V_{ds}, velocity saturation occurs and the DC curves at V_{gs} = 0 V and -1 V are therefore seen to saturate.

Vertical channel JFETs have high-speed switching capabilities due to their unipolar switching nature. In

unipolar switching (i.e., the gate voltage V_{gs} remains less than or equal to zero during switching) no carriers are injected from the gate, hence switching can be performed at high speeds (without charge storage effects). These switching characteristics can be described by the capacitances between the various internal model nodes. The gate-source capacitance can be described with a constant metallization capacitance C_{gsm}, and a voltage-dependent capacitance C_{gsj} due to the gate junction relative to the source. From the gate to drain, there exists a voltage-dependent gate-N- base junction capacitance C_{gdj}.

In the bipolar mode, the gate voltage is positive relative to the source such that the gate-source junction becomes forward biased. The forward-biased junction injects minority carrier holes into the channel, thus reducing the on-state resistance of the device. This gives the device greater power handling capability. The drawback of this configuration is that the driver circuit for the gate becomes more complicated as a high current gate drive capability is required (whereas the unipolar mode is voltage controlled). Therefore, the bipolar mode is not commonly employed for power switching and the majority of applications utilize the unipolar switching mode. However, the bipolar mode is modeled here with the conductivity modulated source region R_{mod}, the modulation current i_{mod}, and the minority carrier lifetime τ [3].

III. CHARACTERIZATION OF SiC JFETs

Bare die research samples from SiCED were used for the high temperature characterization study. The SiC VJFET, usually supplied as a cascode device with a Si MOSFET and packaged in the general plastic IXYS i4 package, has a vertical device topology. The device has a surface area of 2.8 mm^2 with a current rating of 2.5 A (I_{ds}) and a blocking voltage of 1200 V. The JFET bare die was then mounted on a Ni plated JEDEC TO-258 package to enable high temperature operation. Fig. 4 shows the experimental set-up for the JFET characterization.

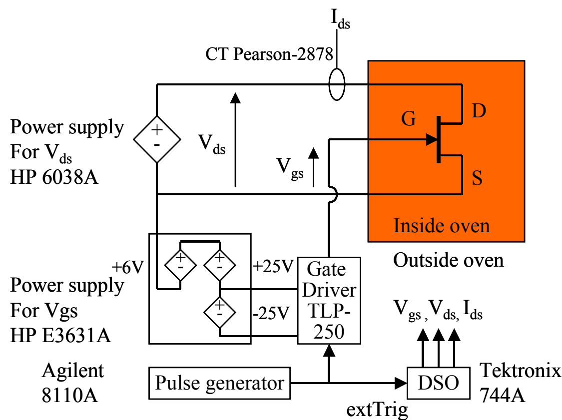

Fig. 4. Experimental set-up for the characterization of SiC JFETs.

The characterization equipment and the power supplies to the device are controlled by a PC with LabVIEW and an IEEE-488 (GPIB) link. The data acquisition procedure was therefore completely automated. There are two power sources used for the characterization; one for the drain–source supply voltage (V_{ds}) and the other for the gate–source supply voltage (V_{gs}). The drain to source voltage, V_{ds} was swept from 0 V to 20 V keeping the V_{gs} constant. V_{gs} was then varied to other values (in constant intervals) and V_{ds} was swept repeatedly to get a family of DC curves. The power supply for V_{gs} outputs two voltage levels. The higher level was used as a parameter that was varied for the DC curves, and the other lower voltage was used to turn-off the JFET. To avoid self-heating, the gate voltage was given in 40 µs pulses from a pulse generator. The gate signal from the pulse generator triggers a digital storage oscilloscope which records the data. This is interfaced to a PC, which then does numerical processing and data storage.

IV. MEASURED AND SIMULATED RESULTS

This paper presents validation data for the model as compared to measured data from SiC SITs obtained from Northrop Grumman and SiC JFET structures from SiCED (cascode structures).

As seen in the on-state curves at 25°C and 100°C (Figs. 5 and 6), the model accurately replicates the four regions of operation as explained before. The model was tested and validated for different gate voltages ranging from 0 V to -4 V. When the gate voltage is negative, the device is in the unipolar mode, the prevalent mode for power switches. Moreover, the gate control circuitry is much simpler for the unipolar mode.

The circuit used in the simulation for the transient response is shown in Fig. 9. It closely emulates the actual test circuit using a gate driver that switches from -16 V to 0 V for the SIT (-20 V to 0 V for the JFET), a small gate inductance, L_g = 1 nH, a drain series resistor, R_L = 100 Ω, a drain series inductance, L_L = 1 nH, packages capacitances, C_{pk} = 2 pf, and a drain supply voltage of 100 V. The gate resistance, R_g was varied (680 Ω, 1.2 kΩ and 3.6 kΩ for the SIT and 0 Ω and 1 kΩ for the SiCED JFET) to provide different turn-on speeds for the devices. Validation results for the switching characteristics of the compact JFET/SIT model are indicated in Figs. 11 and 12 for the SIT and Fig. 10 for the JFET. In all the figures the measured data is always depicted as the solid curve while the model is indicated as a dashed curve. Fig. 11 shows the drain voltage $V_{ds,}$ drain current I_{ds}, gate voltage V_{gs}, and gate current I_{gs} at 25°C. Fig. 12 shows the same waveforms for 100°C. A comparison of the two sets of waveforms shows that there is no considerable change in the switching time of the device even at a higher operating temperature. Fig. 10 shows the V_{ds}, I_{ds}, and V_{gs} turn-on waveforms at 25°C for the SiCED JFET.

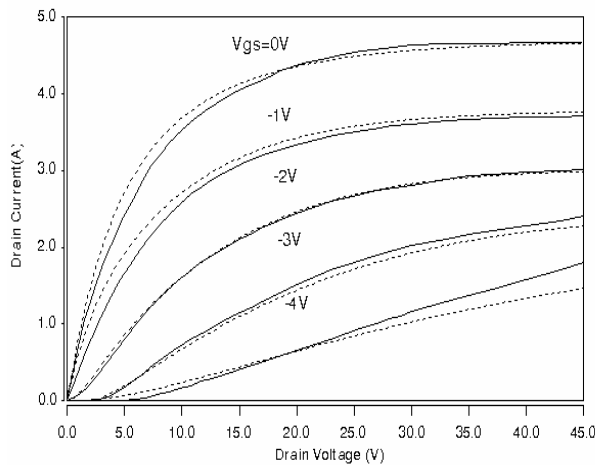

Fig. 5. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 25°C for different gate voltages.

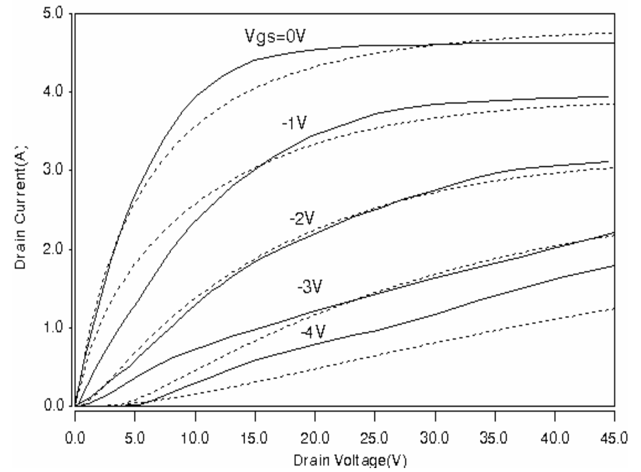

Fig. 6. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 100°C for different gate voltages.

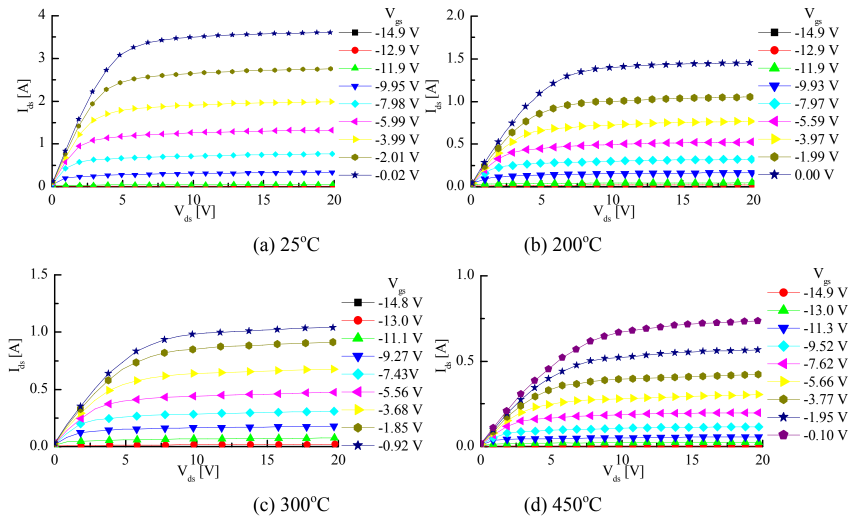

Fig. 7. DC characteristics of the SiC JFET as function of V_{gs}.

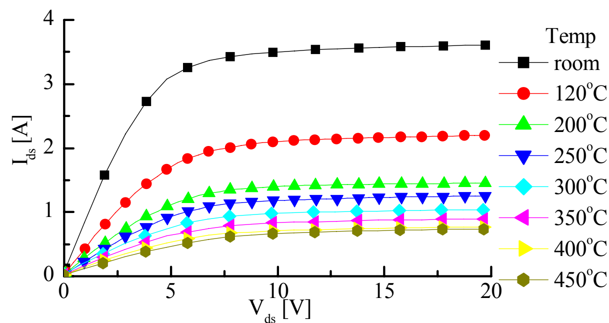

Fig. 8. Temperature dependency of the DC characteristics of the SiC JFET for V_{gs} = 0 V.

The unipolar switching characteristics of the device can be described by the capacitances listed in Table II. For the case of the turn-on waveforms in Figs. 11 and 12, the gate voltage waveform is described by a two-phase capacitive response. During the initial rise of the gate voltage, the constant C_{gsm} and small junction capacitance C_{gsj} are charged yielding the initial slope in V_{gs}. The effect of C_{gsm} and C_{gsj} charging are also seen in the I_{gs} curves and have consequently been modeled.

The transient waveforms for the JFET seen in Fig. 10 have been modeled with the same equations that were used for the SIT. But, it can be clearly seen that there is a considerable delay for I_{ds} to switch from 0 A to 1 A. This is attributed to the parasitic capacitance in the cascode structure due to the presence of the MOSFET.

Fig. 7 illustrates the I_{ds}-V_{ds} characteristics of a SiC JFET with the gate voltage V_{gs} as a parameter at 25°C, 200°C, 300°C and 450°C ambient temperatures, respectively. The JFETs are seen to have pentode-like characteristics with a threshold voltage of V_{gs} = -12 V. The saturation current at room temperature is 3.5 A, and the on resistance was found to be 1.33 Ω. As the temperature increases, the threshold voltage also changes. At 200°C, 300°C and 450°C, the threshold voltages were found to be -13 V, -14 V and -15 V respectively. At 450°C, the pentode-like characteristics of the JFET slightly change to triode-like behavior. The saturation current in this case becomes 0.7 A, which is only 20% of that at room temperature and the drain-source resistance increases to as much as 10.0 Ω in the linear region for V_{gs} = 0 V. Fig. 8 shows the DC characteristics at V_{gs} = 0V for different ambient temperatures. The saturation current was seen to decrease in accordance with increasing temperatures from 3.5 A at 25°C to a mere 0.7 A at 450°C. It can also be clearly seen that, for an operating current of 0.5 A, the voltage drop between the drain and source changes from 0.7 V at room temperature to 6 V at 450°C. This shows that that conduction losses at 450°C is a magnitude higher than at room temperature.

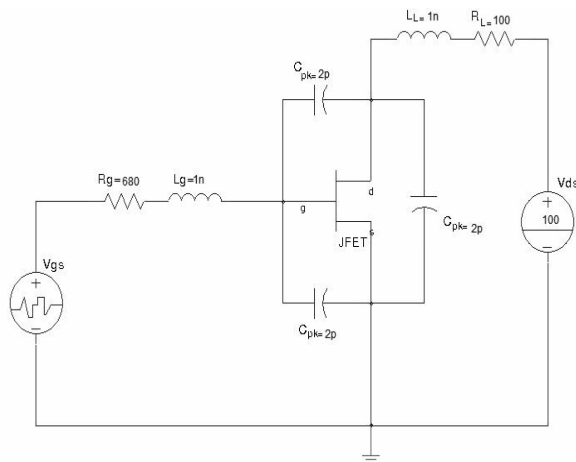

Fig. 9. Simulation test bench for the transient analysis of the SiC SIT/JFET

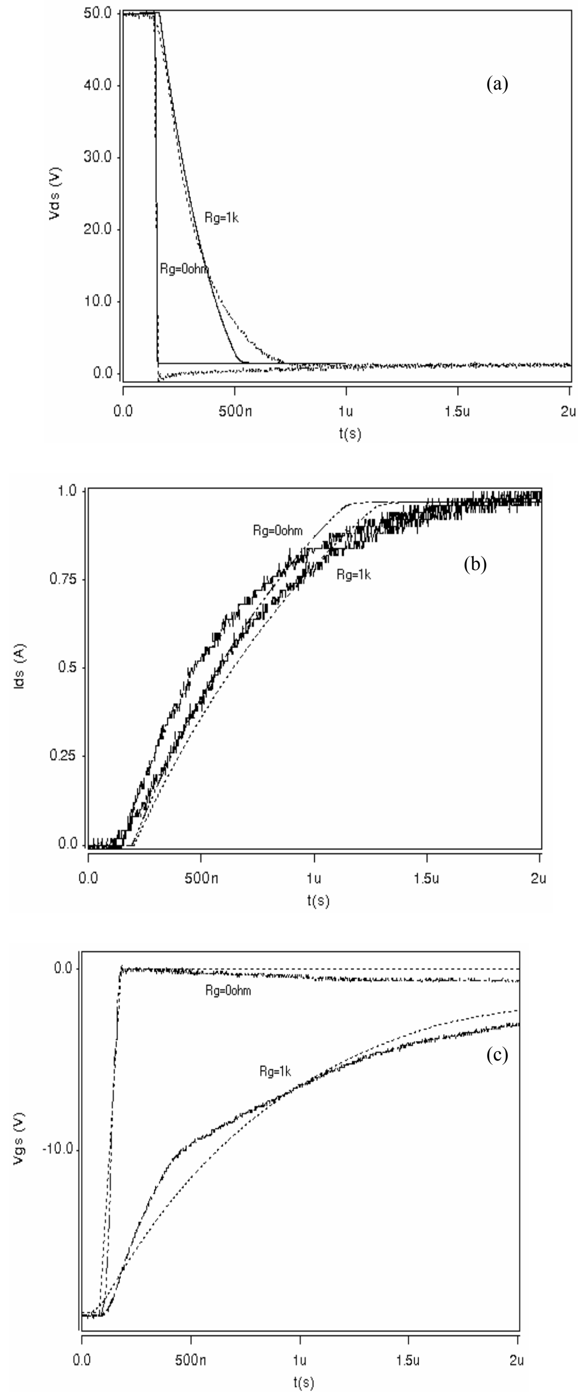

Fig. 10. Silicon carbide JFET simulated (dashed) and measured (solid) turn-on waveforms at 25°C; a) drain voltage, b) drain current, and c) gate voltage.

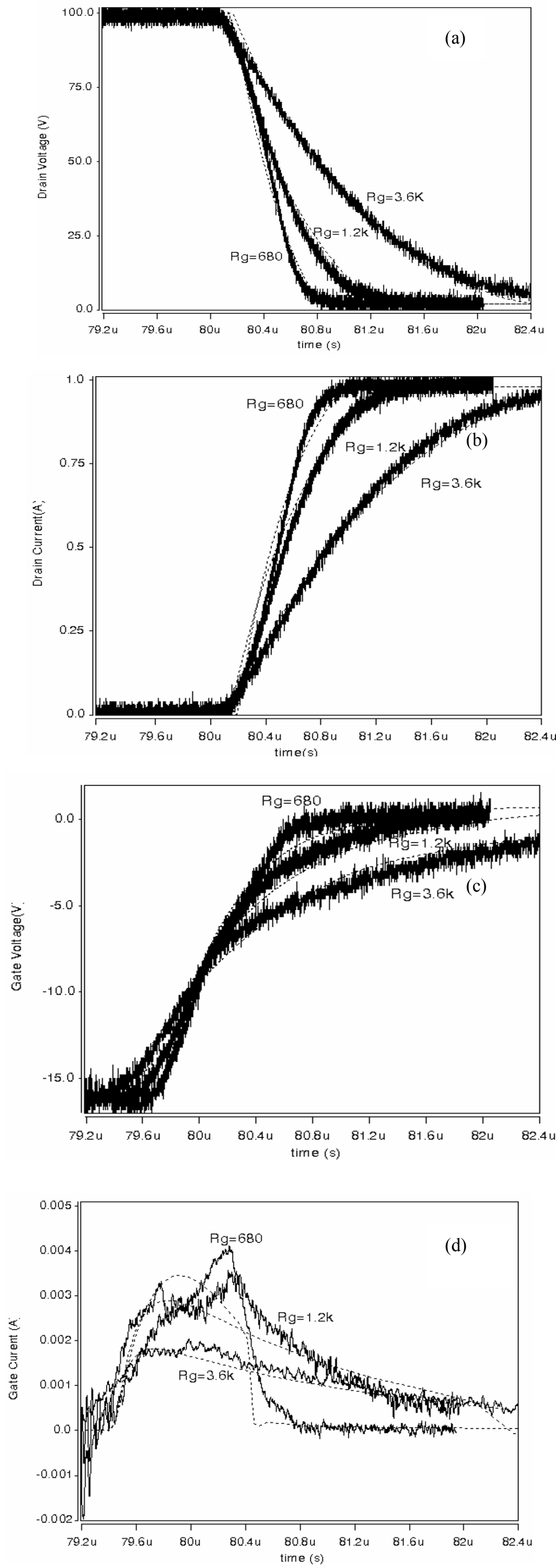

Fig. 11. Silicon carbide SIT simulated (dashed) and measured (solid) turn-on waveforms at 25°C; a) drain voltage, b) drain current, c) gate voltage and d) gate current for different gate resistances.

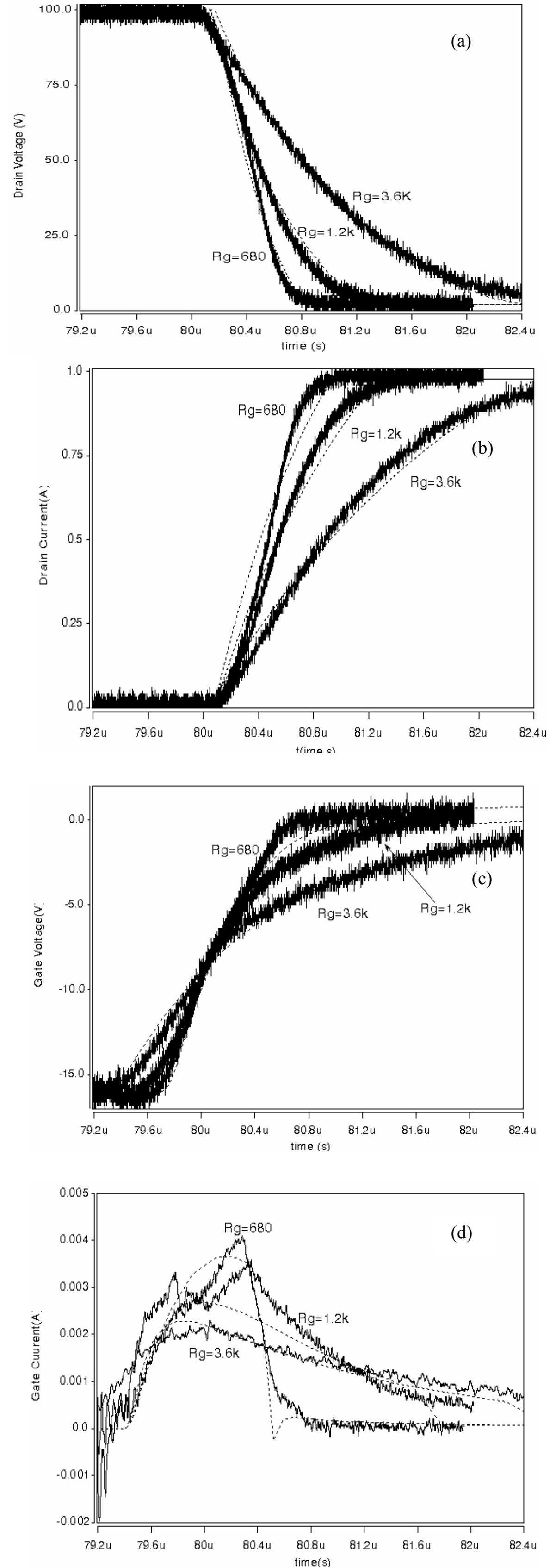

Fig. 12. Silicon carbide SIT simulated (dashed) and measured (solid) turn-on waveforms at 100°C; a) drain voltage, b) drain current, c) gate voltage and d)gate current for different gate resistances.

V. CONCLUSION

A compact SiC power JFET/SIT model has been developed and demonstrated for use in circuit simulators. The model is a combination of empirical relations for on-state behavior, and temperature and material based device physics equations that accurately replicate the transient behavior of the device. The model was shown here to accurately describe the on-state and transient characteristics at 25°C and 100°C for the SIT. The SiC JFET has also been successfully modeled as seen in the transient curves for the same. SiC JFETs from SiCED were also characterized from 25°C to 450°C. It was found that the maximum current at 450°C becomes 20% of that of the room temperature current for the same gate and drain bias. The threshold gate voltage was also seen to increase negatively with increasing temperature.

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