Modeling Vertical Channel Junction Field Effect Devices in Silicon Carbide

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***Abstract*- The electrical characterization and model development for silicon carbide (SiC) vertical channel SIT and JFET structures are presented in this work. A compact model is developed based on the device geometry and SiC material properties. The model is validated against measured data at 25°C and 100°C for a prototype 0.03 cm^2 SiC SIT provided by Northrop Grumman. The model's on-state and transient characteristics are validated over this temperature range. Validation of the model shows excellent agreement with measured data. The physics-based approach implemented in this model is crucial to describing the transient behavior over a wide range of application conditions and temperature ranges.**

NOMENCLATURE

A_g	Gate-drain overlap area (cm^2)
A_s	Gate-source overlap area (cm^2)
α	Thermionic emission factor
C_{gd}	Gate-drain depletion capacitance (F)
C_{gs}	Gate-source depletion capacitance (F)
C_{gsm}	Gate-source metallization capacitance (F)
ε_{SiC}	Dielectric constant of silicon carbide (F/cm)
f_{csj}	Gate-source area factor
i_o	Channel current factor (A)
I_{jfet}	JFET channel current (A)
i_{mod}	Conductivity modulated current (A)
I_{sgd}	Gate-drain junction saturation current (A)
I_{sgs}	Gate-source junction saturation current (A)
k	Boltzmann's constant (J/K)
λ	Channel modulation parameter
N_b	Base dopant density (cm^{-3})
N_{gd}	Emission coefficient for gate-drain junction
N_{gs}	Emission coefficient for gate-source junction
P_1	Power factor coefficient
q	Fundamental electronic charge (C)
R_{mod}	Zero bias value of intrinsic region resistance (Ω)
R_d	Variable drift resistance (Ω)
R_m	Series contact resistance (Ω)
τ	Carrier lifetime (s)
V_{bi}	Built-in junction potential (V)
V_{ds}	JFET channel voltage (V)
V_{gs}	Gate-source voltage (V)
V_{gd}	Gate-drain voltage (V)
V_p	Channel pinch-off voltage (V)
V_t	Thermal voltage (V)
W_{bz}	Zero-bias base width (cm)
W_{gd}	Depletion width of gate-drain area (cm)

I. INTRODUCTION

Silicon carbide (SiC) power devices are expected to show superior performance compared to other semiconductor materials primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and higher temperature capability than conventional Si materials [1]. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices, the combination of $1/10^{th}$ the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed.

Of all SiC power transistors (e.g., MOSFETs, JFETs, BJTs) currently under development, SiC JFETs have perhaps the greatest near term potential for commercialization for high temperature applications. SiCED/Infineon in Europe and Semisouth Laboratories [10] in the U.S. are two companies actively working toward this end. The availability of compact circuit simulation models for these devices will greatly aid power electronics engineers in circuit design, testing, prototyping, and product development. Presently, validated SiC power diode and MOSFET models exist that accurately describe on-state and switching conditions over a wide range of application conditions and operating temperatures [2]-[4]. The work shown here extends the previous modeling work to vertical channel junction field effect transistor (JFET) behavior. Such behavior is present in both power JFETs and static induction transistors (SITs), since their structures are very similar. In fact, the primary difference in the structures is the spacing of the gate contacts (more tightly spaced in SITs), and gate implant depths (shallower for SITs). In this paper a compact circuit simulator model has been developed for SiC JFET/SIT structures [5] as shown in Fig. 1. The model accurately describes device performance for on-state and switching characteristics for 25°C and 100°C.

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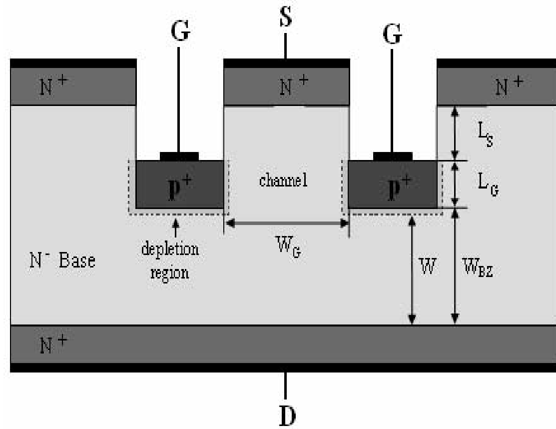

Fig. 1. Cross-sectional structure of SiC vertical JFET/SIT.

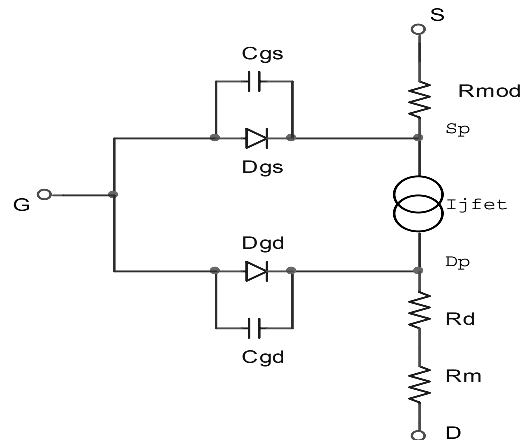

Fig. 2. Internal model topology of the SiC JFET/SIT.

TABLE I. JFET MODEL EQUATIONS

JFET/SIT channel currents

$I_g + I_d = I_s$

$if\ V_{ds}>=0$

$I_{jfet}= i_o\cdot[1+\tanh\{P_1(V_{gs}-V_p)\}]\cdot\tanh(\alpha V_{ds})\cdot e^{\lambda V_{ds}}$

$P_1 = 1 + 0.05(V_{gs})$

On-State Equations

$W = W_{bz} - W_{gd}$

$$R_d = \frac{W}{qN_b\mu_n(A_g + A_s)}$$

$$\mu_n = \frac{947}{1+(\frac{N_b}{1.94x10^{17}})}(\frac{T}{300})^{-2.15}$$

$q_m = \tau \cdot I_{gs}$

$$i_{\mathrm{mod}} = \frac{(\mu_n + \mu_p)V_{gs}q_m}{W_{gd}^{\ 2}}$$

$I_{gd} = I_{sgd}(exp(V_{gs}/ngs\cdot V_t)-1)$

$I_{gs} = I_{sgs}(exp(V_{gd}/ngs\cdot V_t)-1)$

Transient Equations

$$W_{gs} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gs}+V_{bi})}{qN_b}}$$

$$C_{gs} = \frac{f_{csj}A_s\varepsilon_{SiC}}{W_{gs}}$$

$$W_{gd} = \sqrt{\frac{2\varepsilon_{SiC}(V_{gd}+V_{bi})}{qN_b}}$$

$$C_{gd} = \frac{A_g\varepsilon_{SiC}}{W_{gd}}$$

II. DESCRIPTION OF THE COMPACT JFET MODEL

Table I lists the equations that comprise the JFET/SIT model presented here. The equations listed in Table I are implemented in the MAST hardware description language and were simulated in the Saber circuit simulator [6] in order to validate the model. The model topology is shown in Fig. 2 and it clearly identifies all the elements that are modeled. Extracted model parameters at 25°C are shown in Table II. The model can be visualized as consisting of a source region resistance R_{mod} that is conductivity modulated by i_{mod} for positive gate voltages with respect to the source, an ideal JFET that describes the channel current I_{jfet}, a bias-dependent series base or drift region resistance R_d, and a series contact resistance R_m.

Structures like those in Fig. 1 exhibit two distinct modes of conduction, unipolar and bipolar. In the unipolar mode, the JFET acts as a majority carrier device, where electrons flow from the source to the drain. For the cross-section shown in Fig. 1, there is a depletion region at the gate-N- base layer interface from either a p-n or Schottky metal junction depending on the gate configuration. The on-state characteristics are dependent on the gate region design; specifically the channel width W_G and gate implant depth L_G [7], as illustrated in Fig. 1. Depending on the gate depth in relation to the channel width, the structure can produce FET-like “pentode” characteristics (long gate depths L_G), diode-like “triode” characteristics (short gate depths L_G), or a combination of pentode and triode characteristics referred

to as "mixed-mode" characteristics (intermediate gate depths L_G). For devices optimized for power switching applications, the device typically exhibits mixed-mode characteristics [7]. For sufficiently negative gate voltages when the channel is "pinched off" due to the intersecting depletion regions, the mixed-mode characteristics may be described by the thermionic emission theory when the device operates in triode region at low currents. Whether this phenomenon manifests itself is a function of the gate spacing or channel width W_G. As V_{ds} is increased, these structures produce the typical linear and saturation regions.

The mixed mode characteristics of this structure can be broken into four regions of operation – (i) ohmic (ii) thermionic (iii) space charge limited current (SCLC) and (iv) SCLC with velocity saturation (V_{sat}) [8] depending on the gate design. Ohmic behavior is seen for less negative values of V_{gs} and thermionic effects are more dominant for more negative gate biases.

TABLE II. MODEL PARAMETERS AT 25°C

Parameter	Value
Vp	6 V
Wbz	100.0×10^{-4}cm
As	0.015 cm^2
Ag	0.015 cm^2
fcsj	0.2
Nb	2.0×10^{15} cm^{-3}
Isgs	1.0×10^{-35}A
Ngs	2
Isgd	1.0×10^{-35}A
Ngd	2
io	4.2×10^7
Vbi	2.8 V
Rm	0.1 Ω
Rmod	0.5 Ω
Tau	0 ns
Lambda	5.0×10^{-4}

The model presented in this paper utilizes a semi-empirical approach for the on-state modeling [9] – [10] and traditional device physics relations for the transient model. The various mathematical relations used in the model are listed in Table I. The equation for the on-state modeling uses a hyperbolic tangent function that contains empirical parameters. The channel current factor i_o can be varied to adjust the absolute current level in the device. The model also has empirically determined polynomial relations *c* and *d*, which are used to adjust the slope of the resulting current. The above-mentioned variables (α, *c* and *d*) are functions of V_{gs}. The thermionic emission factor α is an empirical relation that determines the amount of thermionic emission current in the model. The thermionic emission factor α also has a temperature dependency that allows the user to model the device for a range of temperatures. It is also observed that a single current equation is able to accurately describe all the different effects in the on-state. This provides better convergence in the simulator as piecewise defined equations are avoided.

Fig. 3 shows the on-state response at 25°C and Fig. 4 shows the same at 100°C. The DC curves show the four regions of operation that manifest in the SIT. In Fig. 3, for the V_{gs}=0 V and -1 V curves, I_{ds} is clearly ohmic until about 5V and then the space charge limited current dominates. For lower V_{gs} values, the thermionic effect (similar to diode action) can be seen before the SCLC. At high values of V_{ds}, velocity saturation occurs and the DC curves at V_{gs} = 0 V and -1 V are therefore seen to saturate.

Vertical channel JFETs have high-speed switching capabilities due to their unipolar switching nature. In unipolar switching (i.e., the gate voltage V_{gs} remains less than or equal to zero during switching) no carriers are injected from the gate, hence switching can be performed at high speeds (without charge storage effects). These switching characteristics can be described by the capacitances between the various internal model nodes. The gate-source capacitance can be described with a constant metallization capacitance C_{gsm}, and a voltage-dependent capacitance C_{gsj} due to the gate junction relative to the source. From the gate to drain, there exists a voltage-dependent gate-N- base junction capacitance C_{gdj}.

In the bipolar mode, the gate voltage is positive relative to the source such that the gate-source junction becomes forward biased. The forward-biased junction injects minority carrier holes into the channel, thus reducing the on-state resistance of the device. This gives the device greater power handling capability. The drawback of this configuration is that the driver circuit for the gate becomes more complicated as a high current gate drive capability is required (whereas the unipolar mode is voltage controlled). Therefore, the bipolar mode is not commonly employed for power switching and the majority of applications utilize the unipolar switching mode. However, the bipolar mode is modeled here with the conductivity modulated source region R_{mod}, the modulation current i_{mod}, and the minority carrier lifetime τ [3].

III. MEASURED AND SIMULATED RESULTS

This paper presents validation data for the model as compared to measured data from SiC SITs obtained from Northrop Grumman. Ongoing work is currently focusing on measured results of power JFET structures.

As seen in the on-state curves at 25°C and 100°C (Figs. 3 and 4), the model accurately replicates the four regions of operation as explained before. The model was tested and validated for different gate voltages ranging from 0 V to -4 V. When the gate voltage is negative, the device is in the unipolar mode, the prevalent mode for power switches. Moreover, the gate control circuitry is much simpler for the unipolar mode.

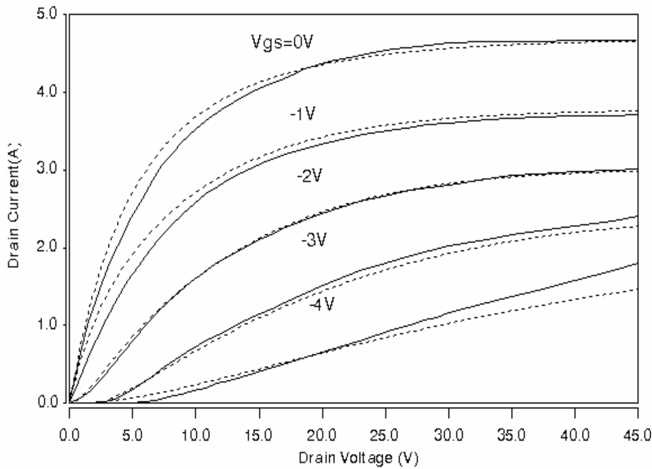

Fig. 3. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 25°C for different gate voltages.

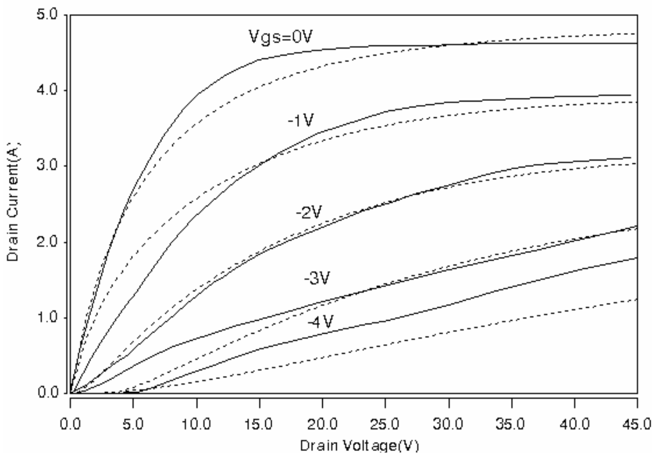

Fig. 4. Silicon carbide JFET simulated (dashed) and measured (solid) on-state waveforms at 100°C for different gate voltages.

The circuit used in the simulation for the transient response is shown in Fig. 5. It closely emulates the actual test circuit using a gate driver that switches from -16 V to 0 V, a small gate inductance, L_g = 1 nH, a drain series resistor, R_L = 100 Ω, a drain series inductance, L_L = 1 nH, packages capacitances, C_{pk} = 2pf, and a drain supply voltage of 100 V. The gate resistance, R_g was varied (680 Ω, 1.2 kΩ and 3.6 kΩ) to provide different turn-on speeds for the devices. Validation results for the switching characteristics of the compact JFET/SIT model are indicated in Figs. 6 and 7. In both of these figures the measured data is always depicted as the solid curve while the model is indicated as a dashed curve. Fig. 6 shows the drain voltage V_{ds}, drain current I_{ds}, gate voltage V_{gs}, and gate current I_{gs} at 25°C. Fig. 7 shows the same waveforms for 100°C. A comparison of the two sets of waveforms shows that there is no considerable change in the switching time of the device even at a higher operating temperature.

The unipolar switching characteristics of the device can be described by the capacitances listed in Table I. For the case of the turn-on waveforms in Figs. 6 and 7, the gate voltage waveform is described by a two-phase capacitive response. During the initial rise of the gate voltage, the constant C_{gsm} and small junction capacitance C_{gsj} are charged yielding the initial slope in V_{gs}. The effect of C_{gsm} and C_{gsj} charging are also seen in the I_{gs} curves and have consequently been modeled.

Once the gate-source capacitance is charged, V_{gs} rises according to the larger gate-drain depletion capacitance C_{gdj}. The gate-drain capacitance C_{gdj} is charged until the threshold voltage V_t (V_t=V_p-V_{bi}) is reached, at which point the drain current flows as C_{gdj} continues charging. The higher the gate resistance, the more time it takes to charge the capacitances and therefore, the switching response gets slower as the gate resistance increases. As observed in the transient modeling results, the switching time is on the order of 0.6 µs (for 680 Ω) and the various depletion capacitances described in the model are able to accurately predict the switching characteristics of the SiC SIT.

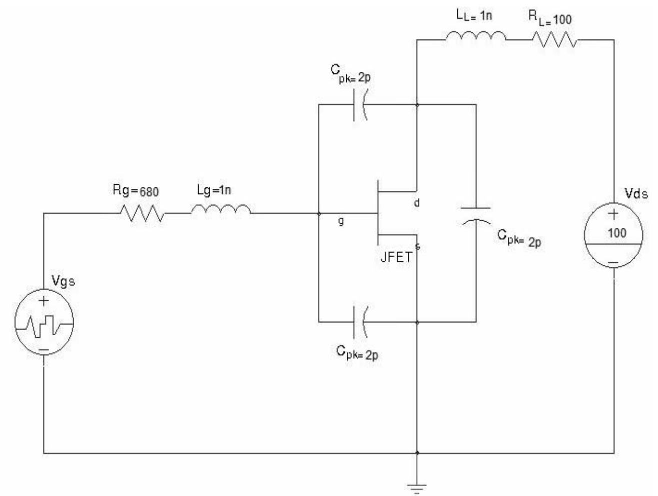

Fig. 5. Simulation test bench for the transient analysis of the SiC JFET.

IV. Conclusion

A compact SiC power JFET/SIT model has been developed and demonstrated for use in circuit simulators. The model is a combination of empirical relations for on-state behavior, and temperature and material based device physics equations that accurately replicate the transient behavior of the device. The model was shown here to accurately describe the on-state and transient characteristics at 25°C and 100°C. Future work will involve characterization of the model against JFET devices from SemiSouth Laboratories. Also, a unified physics-based model for SIT on-state behavior is under investigation.

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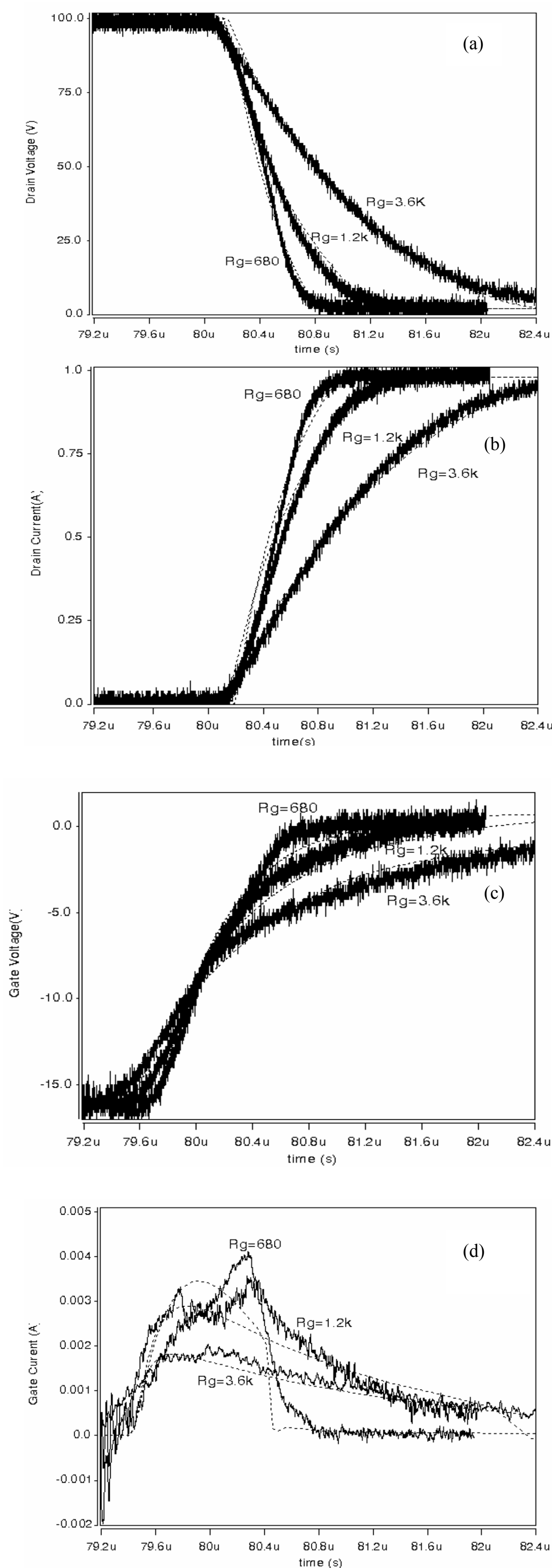

Fig. 6. Silicon carbide JFET simulated (dashed) and measured (solid) turn-on waveforms at 25°C; a) drain voltage, b) drain current, c) gate voltage and d) gate current for different gate resistances.

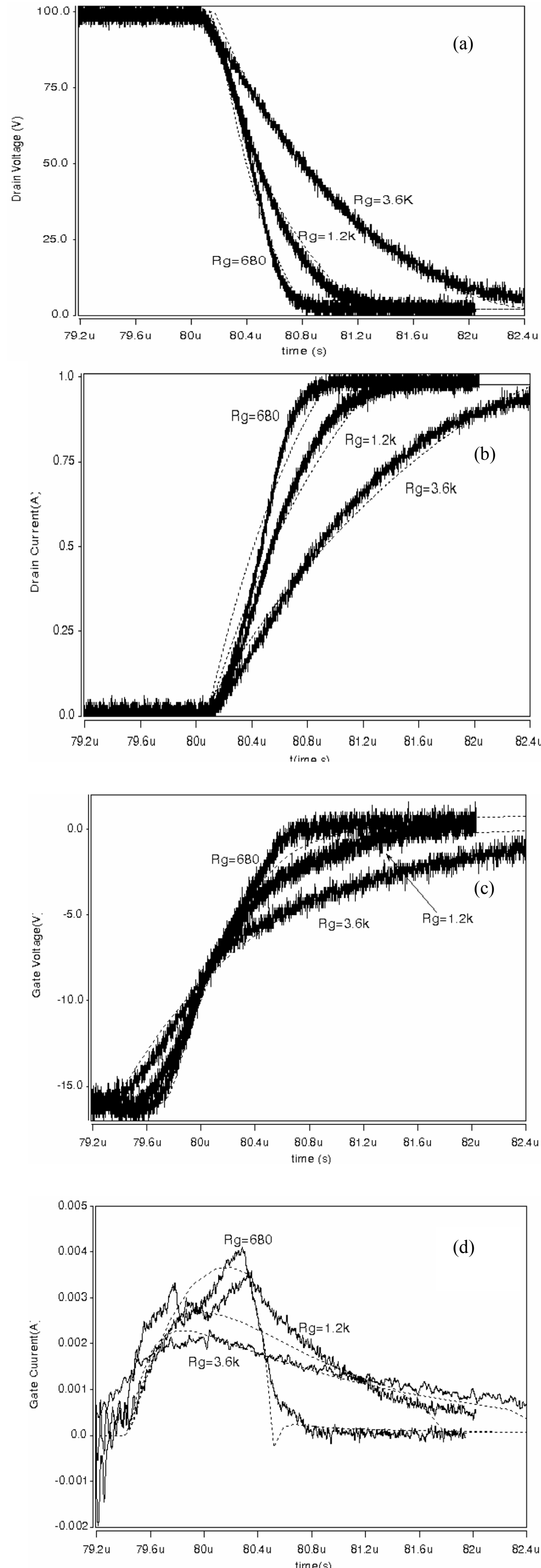

Fig. 7. Silicon carbide JFET simulated (dashed) and measured (solid) turn-on waveforms at 100°C; a) drain voltage, b) drain current, c) gate voltage and d)gate current for different gate resistances.

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