

Testing and Modeling Electrical Characteristics of Novel Silicon Carbide (SiC) Static Induction Transistors (SITs)

Avinash S. Kashyap, Sharmila D. Magan Lal,
Ty R. McNutt, Alexander B. Lostetter, Alan H. Mantooth

Silicon Carbide Research Group
Department of Electrical Engineering
University of Arkansas
3217 Bell Engineering Center
Fayetteville, AR 72701

Abstract

Over recent years, there has been a steady increase into the research of Silicon Carbide (SiC) based device technology for high power and high temperature applications. Experimental SiC static induction transistors (SITs), obtained through Northrop Grumman and the United States Air Force, are some of the power devices that are currently under characterization by the University of Arkansas SiC Device Modeling Group and will be explained in this paper. SITs have several major advantages: high power, high speed, low noise, and negative current/temperature characteristics. By building basic switching circuits, characteristics such as drain to source on resistance, voltage amplification rate, mutual conductance, and response times are being acquired. Compact circuit simulation models utilizing these measured characteristics are under development for the SIT so that they can be made available in commercial simulators. The current modeling work is being performed in the MAST HDL, but the in-house Paragon package will be utilized to generate the model code in VHDL-AMS, as it will become the future standard. The models are being validated by actual device measurements and key power electronic applications for the devices are also under development.

Introduction

The static induction transistor (SIT) was invented by Professor Junichi Nishizawa of Tohoku University in 1950 [1]. By 1969, it became a complete device having non-saturating type voltage/current characteristics. One of the main advantages of the SIT device is its high speed switching characteristics. Since no carriers are injected from the gate, switching can be performed at an extremely high speed (without storage effects) and a small gate resistance (r_g) is used for minimum high frequency signal loss. SITs have

high input impedance and is a voltage controlled device and therefore low drive power is required at the gate. The absence of electric current concentrations for very high breakdown voltage resistance can be explained by the negative temperature coefficient of the drain current, due to some residual channel resistance, which makes it difficult for thermal runaway to occur. Thus SiC SITs are highly suited for high power applications. The non-saturating current/voltage characteristic is based on the SIT exponential function characteristics due to their reduced negative feedback capacitance [1].

SITs can be defined as a type of v-channel field effect transistor (FET) in which the distance between the source and depletion layer of the drain is so reduced that the negative feedback of the channel resistance will not affect the direct current characteristics. SITs require a negative voltage signal in order to turn off as they are normally-on devices. SiC SITs have very compelling applications mainly in the power and aerospace industry due to their high-temperature and high-current handling capabilities [2].

Operation of SITs

The SIT can operate as a unipolar or bipolar device. Figure 1 shows the unipolar mode of the SIT. In this mode, the SIT acts as a majority carrier (electrons) device. The electrons are the only means of current flow. Consider an n-channel device in which the drain and source are shorted. There is a depletion in the interface and when a voltage is applied across drain and source, the majority carriers are transported from source to drain. Calculation of the built in potential of the depletion region can be done using the following relation:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad \text{Equation (1)}$$

The depletion region continues to increase as the negative voltage is applied. The channel width is consequently reduced and the channel length is increased. This causes the on-resistance to increase as the flow of electrons is restricted. When the reverse voltage is very large, the depletion region grows large enough to meet, thereby “pinching off” the flow of current as shown in Figure 2.

In the bipolar mode of operation, the gate-source region is forward biased, which in effect is turning on the pn-junction (a diode) into conduction mode between the p^+ and n^- region. As a result, electrons are injected into the body of the device and the channel, reducing the on-resistance. Both electrons and holes conduct resulting in a bipolar mode as seen in Figure 3.

When V_{DS} is very high, the depletion region does not grow parallel as illustrated in the previous cases. It grows more at the source side than drain. This is due to the fact that resistive voltage drops occur along the length of the channel, distorting the width of the depletion layers. Even if the pinch-off voltage V_P is applied, a certain amount of current will continue to flow. If the device is to be operated under a very high drain to source voltage then it has to be ensured that V_{GS} is more negative than V_P as illustrated in Figure 4 [3].

Generally, the unipolar mode is used for high frequency applications whereas the bipolar mode is utilized for circuits handling high power. Reason being, the bipolar mode requires the removal of minority carriers from the bulk substrate, which takes more time, thus maximum frequency is reduced.

Testing Electrical Characteristics

Currently there are no SiC SITs commercially available, however these components are under research and development by several manufacturers, including Northrop Grumman, Cree, Infineon, and Rockwell. Fortunately, the University of Arkansas (UofA) obtained a few experimental Northrop Grumman static induction transistors and Cree Schottky diodes. The UofA Silicon Carbide group has begun to utilize these components by building a SiC SIT half-bridge as seen in Figure 5.

Figure 6 illustrates the experimentally obtained turn-ON characteristic curves of one of the SIT devices. These SiC SITs were developed by Northrop Grumman for use in low voltage, high frequency radar applications. Note that in this figure the transition region consists of the cut-off area (Off state) and the activation area. When the drain and source junctions are inversely biased, the SIT device is off. The SIT is activated, when the source junction is forward biased and the drain junction is reversed biased. The saturation area (On state) takes place when the gate voltage is made positive or zero resulting in both the drain and source junctions being forward biased [1].

By using a basic switching circuit (as seen in Figure 7) the ON characteristic curves of the SIT device are obtained. Note that the driving circuit in Figure 7 determines the switching speed of the circuit. Also the value R_S is the output resistance in the drive circuit and it is necessary to make R_S small in order to obtain fast switching [4].

Using Ohm's Law and the measurement of V_{DS} vs. I_D for different values of V_{GS} and temperature, the on-resistance can be obtained. For instance, based on the ON characteristic curve in Figure 6, the on-resistance for this SIT device at room temperature

will be 2 Ω . Theoretically, the on-resistance will go down as temperature increases because of the negative current/temperature characteristics.

The voltage amplification rate is the ratio of the potential change of V_{DS} and V_{GS} . By referring back to the ON characteristics curve in Figure 6, an example will be used to illustrate the concept of the voltage amplification rate. The drain to source voltage is measured when the drain current reaches a certain value (i.e. $I_D = 1.5A$) after applying the voltage between the drain and source by making the bias voltage (i.e. $V_{GS} = -1V$), resulting in the value of $V_{DS} = 27V$. Using the formula below:

$$\mu = \left| \frac{V_{DS}}{V_{GS}} \right| \quad \text{Equation (2)}$$

the voltage amplification rate for the above example will be 18.

Another basic circuit, as seen in Figure 8, is under construction in order to determine the mutual conductance of the SIT device. The drain current I_{D1} can be obtained when switch 1 is placed at position 1 and switch 2 is placed in position 2; I_{D2} is obtained when switch 1 is placed at position 2 and switch 2 is placed at position 1. The mutual conductance can then be found by applying the measured values of I_{D1} and I_{D2} into the following formula:

$$g_m = \frac{I_{D1} - I_{D2}}{\Delta V_{GS}} \quad \text{Equation (3)}$$

The SIT's response time (i.e. delay time, rise time, storage time, and fall time) can be obtained by examining the measured input current and voltage versus the output. The delayed time is the time required for the output to reach 10% of the maximum amplitude

starting at the time of the application of the input pulse. The rise time is the time required for the output to go from 10% to 90% of the maximum amplitude. The storage time is the time required for the output to decrease 90% of the maximum amplitude after the input pulse disappears. Finally, the fall time is the time required for the output to decrease from 90% to 10% of the maximum amplitude [1].

Modeling Characteristics

Given the increasing popularity of SiC devices, compact circuit simulation models are in great demand so that commercial simulators can include them in their model libraries. The MSCAD lab at the University of Arkansas uses the MAST Hardware Description Language (HDL) [5] to model these devices. MAST is a flexible language that can be used to generate excellent behavioral models. The model parameters and means of extraction for the SiC SITs have been identified [6]. As stated previously, some of the primary electrical parameters are transconductance (g_m), the drain/source saturation current (I_{Dss}), the threshold voltage (V_t), the lumped resistance parameter (r_s), gate-source junction capacitance at zero bias (c_{gs}), gate-drain junction capacitance at zero bias (c_{gd}). The term g_m is defined as the maximum transconductance at zero voltage and uses a value of I_{Dss} that is average of the current in the saturation region of the device for zero gate voltage. Figure 9 shows the equivalent circuit for the SIT model that can be used for analyses. V_t was extracted from the data using the square-root of the I_D vs. V_{GS} curve, in which the slope of the curve is extrapolated to the x-axis, and V_t is defined as the intercept. V_t is the externally applied voltage to achieve pinch-off. The Lumped resistance parameter (r_s) will be modeled using the EMPEROR technique [7]. The characteristic equations that are used to model the SIT are as follows:

i) *Cut-off region* ($V_{GS} - V_{to} \leq 0$) : $i_d = 0$ Equation (4)

ii) *Linear region* ($0 < V_{DS} < V_{GS} - V_{to}$) : $i_d = g_{ml} V_{DS} * [2(V_{GS} - V_{to}) - V_{DS}]$ Equation (5)

iii) *Saturation region* ($0 < V_{GS} - V_{to} \leq V_{DS}$) : $i_d = g_{ms} * [V_{GS} - V_{to}]^2 * [1 + \xi V_{DS}]$ Equation (6)

where ξ is the pinch-off parameter that has been introduced in the model for modeling the the SIT pinch-off effect. The transconductance of the SITs vary at the active and the saturation regions. These parameters and their extraction aid in making a robust model that can be used extensively in simulators.

Temperature dependent modeling is also needed as the SITs operate at high temperatures (theoretically up to 600 °C). Repeated testing of the SITs at room temperature has already been done at the MSCAD Lab. High-temperature study will be carried out at the HiDEC facility. The models will then be validated with actual device measurements with the SITs provided by the UofA collaborators.

Conclusion

Currently, the SiC research that is being performed by the UofA is increasingly showing the versatility of these wide band gap devices. Before SiC SITs can be commercially launched, issues such as modeling and device physics need to be demonstrated. The characterization study currently under investigation has shown the excellent power density handling capabilities of these devices. The model of the SIT under development will be a very useful tool for power electronic circuit designers. Extensive testing needs to be done to establish the reliability of SITs. The packaging issue for these devices is also being concurrently addressed by the research team.

References

- [1] Tokin SIT Handbook, Tohoku Metal Industries Co., Ltd., Japan
- [2] Neudeck, P.G.; Okojie, R.S.; Liang-Yu Chen “High-temperature electronics - a role for wide bandgap semiconductors?”, Proceedings of the IEEE , Volume: 90 Issue: 6 , Jun 2002 Page(s): 1065 -1076.
- [3] Alex Lostetter, “The Design, Fabrication, and Analysis of Half-Bridge Multichip Power Modules (MCPMs) Utilizing Advanced Laminate, Silicon-Carbide, and Diamond-Like-Carbon Technologies”, Ph.D. Dissertation, University of Arkansas at Fayetteville, May 2003.
- [4] M. Tatsuta, E. Yamanaka, and J. Nishizawa, “High Frequency – High Power Static Induction Transistor”, IEEE Industry Applications Magazine, Volume: 1 Issue: 2, Mar/Apr 1995, Page(s): 40-45.
- [5] Analogly Inc. Application Notes–Model Fundamentals, 1991-1992
- [6] Charles J. Scozzie, C. Wesley Tipton, W. Merle DeLancey, James M. McGarrity, and F. Barry McLean, “High Temperature Stressing of SiC JFETs at 300⁰C”, Reliability Physics Symposium, 1994. 32nd Annual Proceedings., IEEE International, 11-14 April 1994, Page(s) 351-358.
- [7] C.S. Wen, M. Guldahl, L.P. Sadwick, R. Kent, and H. Gaffur, “Measurement and Parameter Extraction of Sub-Micron VLSI MOSFET Test Structures”, Proc. IEEE 1992 Int. Conference on Microelectronic Test Structures, Vol 5, March 1992.

Acknowledgements

The authors gratefully acknowledge the financial support provided by the National Science Foundation (NSF) and Texas Instruments for this project. Gratitude is also given to Northrop-Grumman and the United States Air Force for their donation of the prototype SiC transistors to the UofA research team. The technical support provided by Cree Research and the National Institute of Standards and Technology (NIST) is also greatly appreciated.

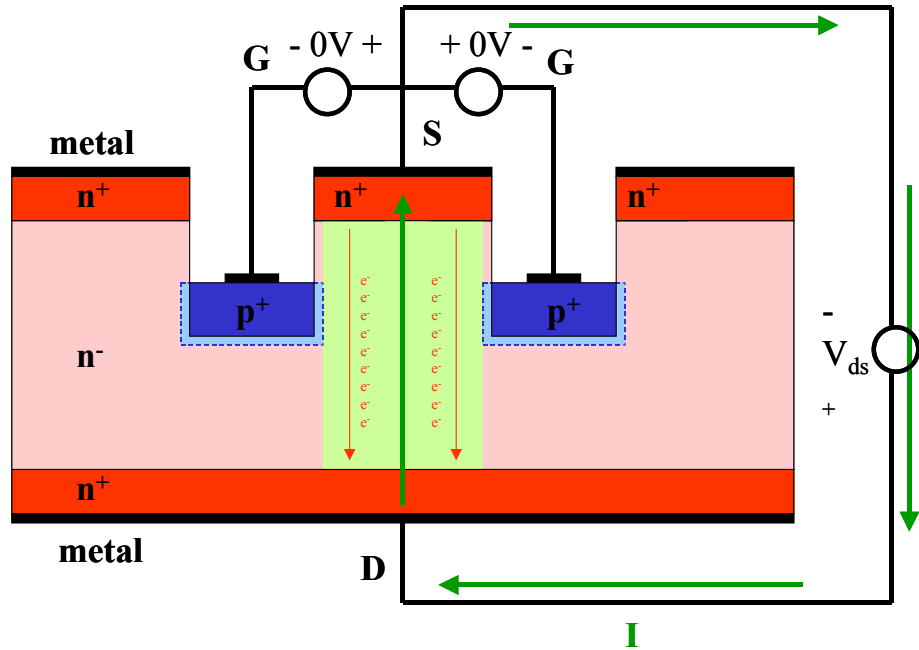


Figure 1. The SIT operating in a unipolar forward conduction mode

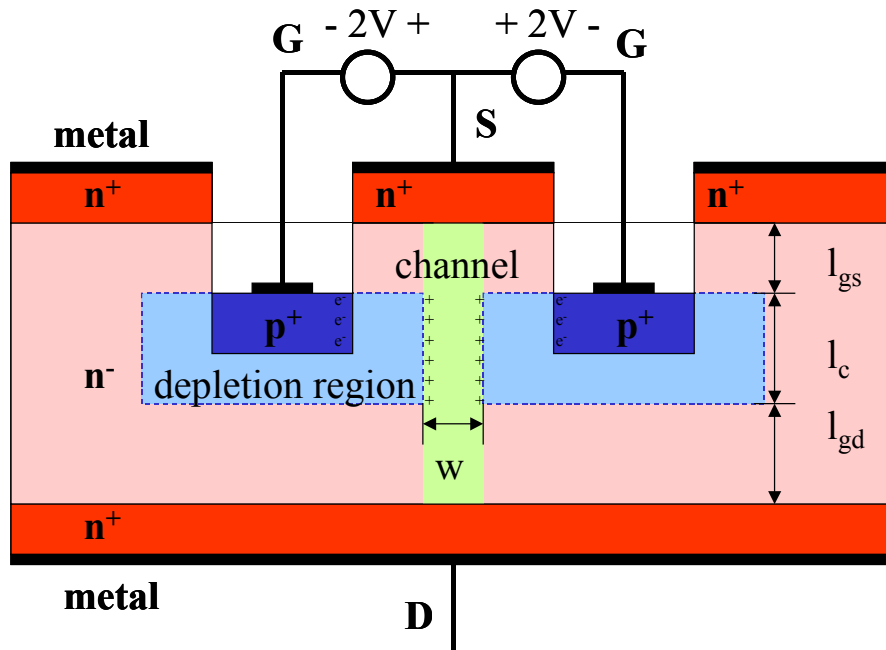


Figure 2. The SIT operating in a reduced forward conduction mode

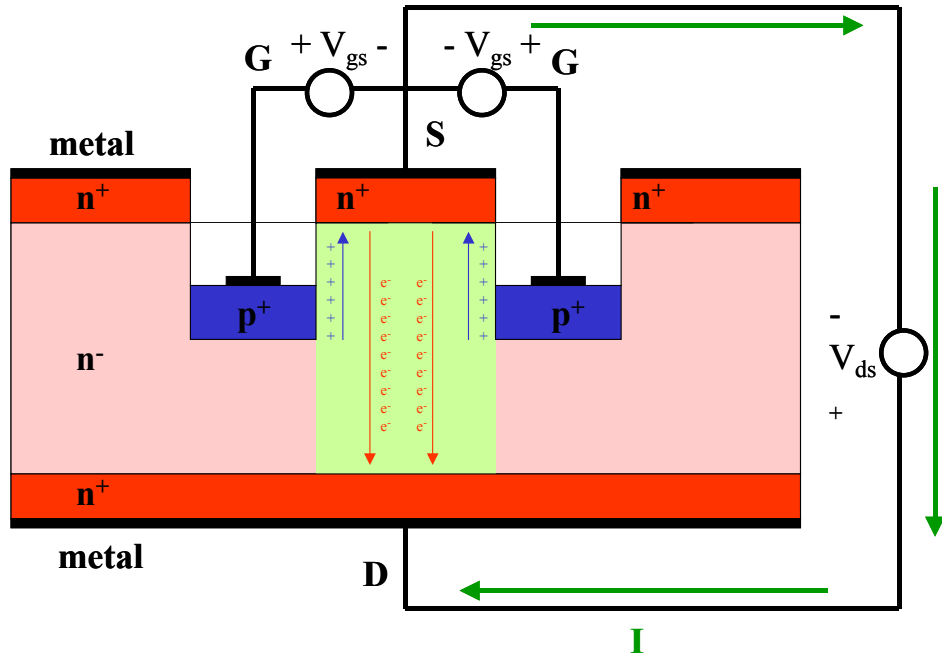


Figure 3. The SIT operating in bipolar mode

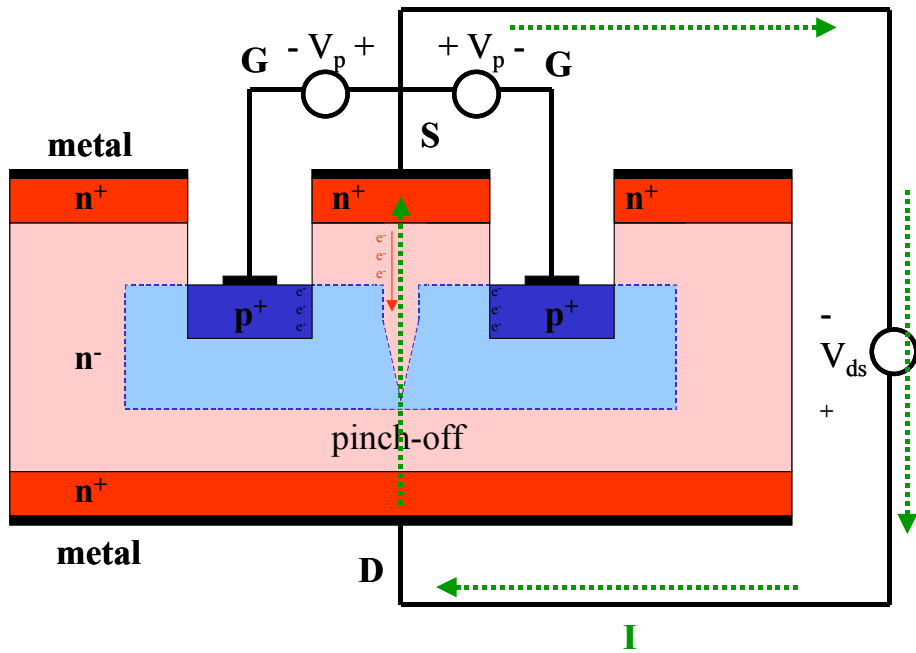


Figure 4. The SIT partially conducting with a large drain to source voltage

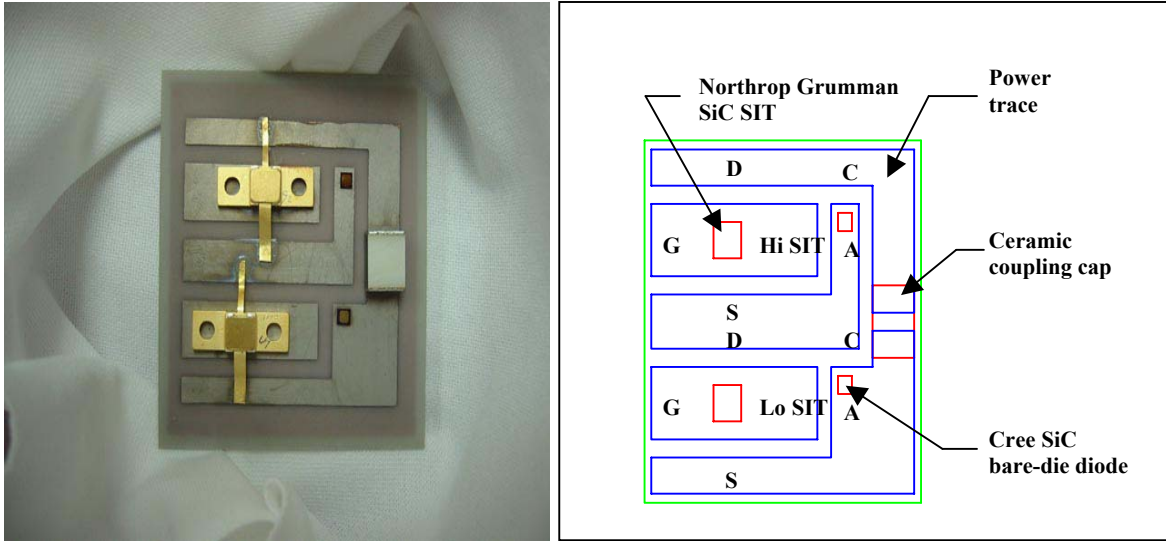


Figure 5. SiC SIT Half-Bridge (500 Watts)

SIT #1203 Device Results

SIT # 1203 I-V Characteristic Curve

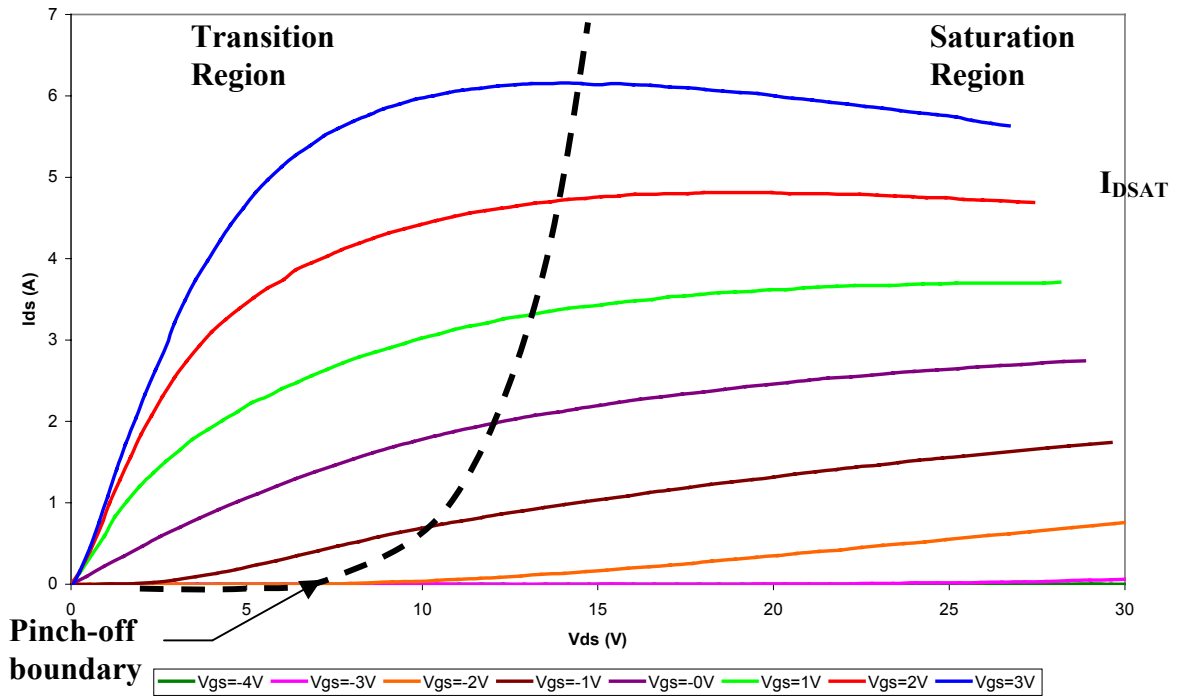


Figure 6. SIT #1203 I-V ON characteristic curve

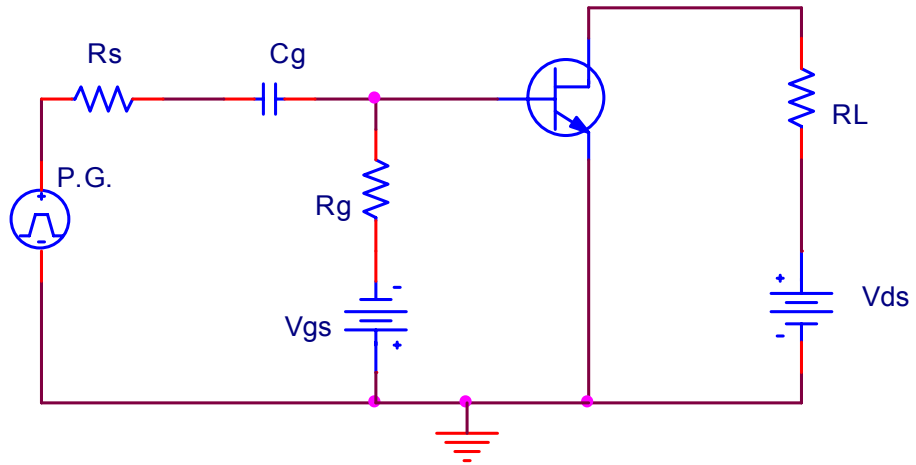


Figure 7. Basic Switching Circuit used to find the On resistance of a SIT

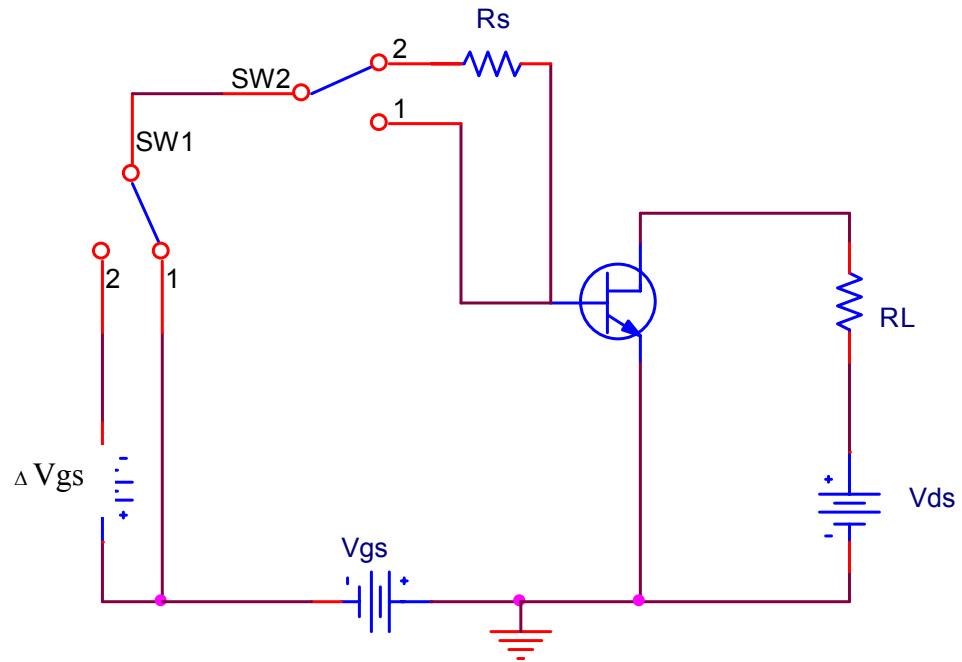


Figure 8. Basic switching circuit used to find the mutual conductance of a SIT

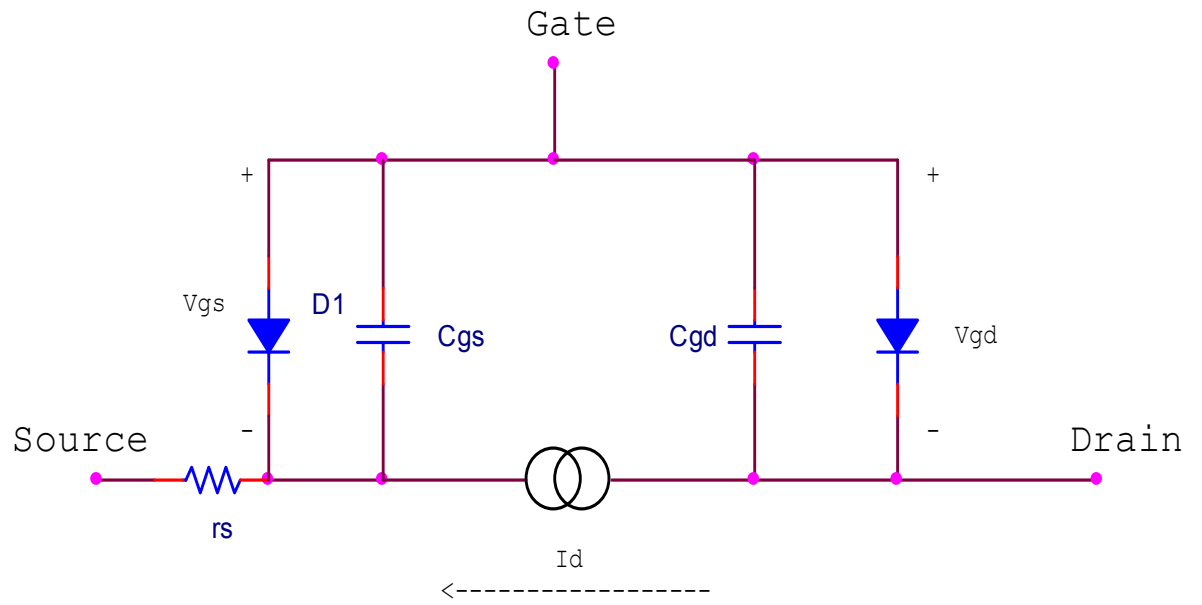


Figure 9. Equivalent circuit for the SIT model