Reliability Concerns in Contemporary SiC Power Devices

Ranbir Singh, Allen R. Hefner, and Ty R. McNutt
National Institute of Standards and Technology
100 Bureau Dr. MS 8120, Gaithersburg, MD 20899. USA
301-975-2077 (ph), 301-948-4081 (fax), ranbir@ieee.org (email).

Despite the remarkable results demonstrated by many groups around the world in exploiting the superior properties of SiC for high power and high temperature devices, there are some seething reliability issues faced by SiC as a material of choice for commercial power devices. Although some of these issues reflect the relative immaturity of this technology requiring years of development, or may be fundamental to this material. This paper attempts to show some of the relevant issues faced by contemporary SiC power devices.

Material defects in present day SiC are the cause of many technological challenges faced by SiC devices. These can be classified into wafer-level defects, and epitaxial-related defects. Wafer-level defects include micropipes (typical density 1-50 /cm^2), closed-core screw dislocations (1000-5000 /cm^2), basal plane dislocations (10^4-10^5 /cm^2) and low angle grain boundaries (10^2-10^3 /cm^2). The affect of these defects on reverse blocking characteristics of devices will be presented at the conference. In the active device regions (epitaxial layers), some of these defects may be annealed if good epitaxial techniques are employed, but others result in (a) reduced critical electric field in devices; (b) higher leakage currents during reverse bias operation; and (c) degradation in the on-state performance of bipolar devices. Although many of these defects affect the reverse characteristics of high voltage SiC devices, long term operation of many devices have revealed that optimally processed devices do not suffer from reliability issues [1,2]. This has allowed for the commercialization of the power SiC Schottky diode. Although the avalanche energy of SiC power devices [3] is experimentally determined to be 3-10X higher than conventional Si power devices because of its larger bandgap and higher thermal conductivity, material defects have been shown to cause filaments that concentrate the plasma of the avalanche current [4].

Detailed experiments conducted recently on bipolar SiC devices have shown that the on-state voltage drop in such devices increases with time when they are kept in the forward biased mode for appreciable length of time. Optical observation of PN diodes undergoing V_F degradation shows a simultaneous formation of mobile and propagating crystal stacking faults. This defect propagates through the entire n- base layer, and act as recombination centers reducing the carrier lifetime in the material, thereby increasing the forward on-state voltage drop [5]. Spectral measurements show that the stacking faults have a primary emission spectrum in the 450 nm peak range [6], and those of threading dislocations is in the 700 nm range. The calculated activation energy for the gliding (propagation) of the partial dislocation that bounds the stacking fault is measured to be in the 0.27 eV range, and the velocity of propagation of defects was $7x10^{-5}$ m/s.

A natural dielectric – SiO_2, is considered a significant advantage for realizing a power MOSFET in SiC, which has great commercial potential. However, there are some significant challenges faced by MOS based devices in SiC. The substantially low MOS channel mobilities [7] achieved in 4H-SiC prevents the realization of the full potential of SiC vis-à-vis Si as a material of choice for medium voltage FETs. Although, a higher gate electric field used in SiC MOSFETs [8] reduces this channel resistance, it substantially worsens the problem of Fowler-

Nordheim tunneling into the gate dielectric. The conduction band offset between SiO_2 and SiC is smaller as compared to that between SiO_2 and Si. Since the tunneling probability of electrons into the gate dielectric is exponentially dependent on the electric field in the gate and temperature, MOS based devices in SiC are expected to have correspondingly lower gate oxide reliability during the on-state operation of MOS devices, for the same operating temperature than Si devices. Another approach investigated extensively is the use of alternative dielectrics with higher dielectric constants [9], which is expected to reduce the electric field in SiC MOS devices. However, many of these materials suffer from correspondingly lower breakdown field strength. A survey of these potential candidates, and results obtained on them will be presented. A high breakdown electric field strength of SiC also affects the choice of passivating dielectrics used in the edge termination and active regions of power devices. Since the electric field in dielectric scale inversely with its dielectric constant, SiO_2 sees a 10X higher electric field during reverse bias operation of these devices, as compared to Si devices. This problem is further exacerbated in trench-gate MOSFETs because of field crowding at trench corners. This is another motivation for exploring high dielectric constant-high dielectric strength materials for SiC power devices.

The higher bandgap of SiC has often been cited as a reason for pursuing high temperature power devices because of their correspondingly lower leakage currents. However, the reverse leakage currents in Schottky-based devices are dominated by the Schottky barrier height of these materials. Since the barrier height of commonly used Schottky metals for SiC devices is in the 0.7-1.2 eV range, the temperature performance of these devices will be similar to Si PN junction-based devices. This problem gets very severe in power MESFETs because the gate regions routinely see a much higher local temperature, as compared to the device ambient temperatures. Another issue that needs substantial research and development relates to the packaging of these high temperature devices. For applications requiring operation beyond 250°C, non-conventional braze materials will have to be investigated because commercial braze materials melt near 280°C. Often some of these non-conventional braze alloys suffer from various practical problems like wetting, flowing and specialized conditions under which they have to be used. Since SiC has a very low coefficient of expansion with temperature, new baseplate alloys should be investigated with close TCE matching to SiC, if these devices have to be operated at higher temperatures. Many ceramic and glass materials used in high voltage packages also suffer from excessive leakage currents when operated beyond 250°C. This also presents a significant challenge for successful exploitation of the high temperature characteristics of some SiC power devices.

While some of these issues presented here are physics-based, many alternative design and technological solutions exist so that many superior properties of SiC can be exploited as a material of choice for power devices. Some of these solutions will be presented at the conference.

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