



Aix-en-Provence, France, 24-26 September 2003

AN SOI CMOS COMPATIBLE THERMAL TRANSDUCER FOR LOW POWER SYSTEMS-ON-A-CHIP DATA ISOLATION

*Ty McNutt, Alexander B. Lostetter, Alan Mantooth, Mohammad Mojarradi**

Dept. of Electrical Engineering, University of Arkansas, Fayetteville, AR, 72701

*Jet Propulsion Laboratory, 4800 Oak Grove, Pasadena, CA 91109

ABSTRACT

An SOI CMOS compatible thermal transducer intended for on-chip data isolation for mixed-signal systems-on-a-chip (SoC) is presented. This device technology is much smaller in size than on-chip inductors and MEMS devices, and requires no post-processing. Further, the device is capable of faster switching speeds (up to an order of magnitude) than equivalent thermal-based MEMS structures due in part to the smaller thermal mass present in the transducer structure. Structure performance was verified using two- and three-dimensional finite-element simulators. Simulation results show that the thermal-based data isolator can propagate a data bit in under a microsecond, while measured results demonstrate a thermal response coupled with an intrinsic device electrical capacitance at frequencies up to 100 kHz.

1. INTRODUCTION

Electrical isolation is utilized to improve the robustness, reliability, and noise immunity of electrical systems. An important requirement of systems-on-a-chip (SoC), with combinations of analog, digital and RF circuitry, is on-chip electrical isolation. Isolation improves the noise performance of the overall system by reducing the coupling between the various technologies. Further, it helps to reduce the chances of cascading failures in a system.

Mixed-signal SoC applications have specific requirements for electrical isolation. First, it is important that the isolation technology be compatible with current CMOS fabrication processes. This typically implies a digital CMOS process that has been enhanced with some analog and RF features such as linear capacitor options, diodes, etc. The isolation technique needs to be as fast as possible. For avionic applications, it is important that the solution be radiation-hardened (rad-hard). Currently available isolation approaches suffer from drawbacks that limit utilization. Optical technologies and proposed MEMS solutions lack the ability to be directly implemented in a standard CMOS or SOI CMOS process and are not rad-hard [1]. Even in specialized processes allowing MEMS, devices such as these are typically

much larger and slower to respond than required [2], [3]. Approaches involving on-chip transformers have yet to perform as desired. On-chip transformers require significant die area, on the order of 100,000 μm^2 , and the circuits used to drive them consume a considerable amount of power. Transformers also produce electromagnetic interference that can adversely affect on-chip signals through substrate coupling.

One solution to a reliable source of on-chip data isolation is a CMOS compatible electrothermal device [4, 5]. One advantage of using thermal as a means of isolation is the current availability of on-chip devices that are able to transmit and receive thermal signals. Also, the thermal-based transducers described here can be made smaller than other isolation technologies, typically around 1,600 μm^2 . Finally, these devices are rad-hard and SOI CMOS compatible. The authors maintain that for low-speed, on-chip applications this isolation device holds promise. While comparisons with other technologies have been drawn to place this work in context, thermal transducers are not proposed as a general alternative to these approaches.

The results presented here are based on isolator designs fabricated in 0.35 μm and 0.8 μm SOI CMOS processes that have approximately 0.4 μm of buried oxide (BOX) and a 0.2 μm Si layer thickness. The BOX, together with the field oxide, is critical to transducer performance. The insulating nature of the BOX prevents thermal energy loss to the substrate, yielding a more intense and focused thermal signal incident on the thermal lens and, therefore, a faster, more efficient device than bulk. Furthermore, SOI technology performs much better in a radiation filled environment compared with bulk CMOS technology. Bulk processes are prone to single-event latchup (SEL), single-event upset (SEU), and other effects caused by particle bombardment. SOI technology is immune to SEL and has proven to be ten times less sensitive to SEU than bulk technology. SOI technology also offers superior temperature performance over bulk, including functionality up to 800 K [6].

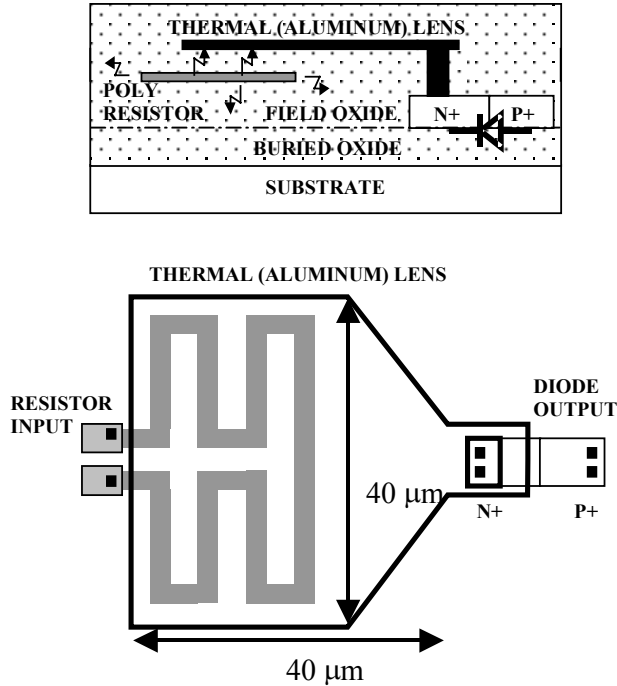


Fig. 1. Cross sectional (above) and top view of SOI CMOS compatible data isolator.

2. THERMAL TRANSDUCER DEVICE STRUCTURE

Fig. 1 shows a cross sectional view followed by a top view of a thermal transducer structure. The transducer structures presented here are approximately 40 μm on a side. The transducer can be decomposed into two sides: the input, or primary side, consisting of a resistor (polysilicon in this illustration); and the output, or secondary side, consisting of a thermal detector (a diode in this illustration). The polysilicon resistor acts as a heater that converts the incident electrical signal to a thermal signal. The diode converts the thermal signal back to an electrical signal. This is accomplished by biasing the detection diode at a constant forward voltage. When the temperature in the diode structure rises, the detected electrical result is an increase in the diode's forward current. The reverse is also true, i.e., the diode could be biased at a constant forward current and a decrease in the diode's forward voltage measured with increasing temperature. The coupling between the primary and secondary side is enhanced through the use of a thermal lens (aluminum in Fig. 1).

The thermal signals generated by the heater propagate outward in all three dimensions. The thermal signal is gathered by the thermal lens and directed toward a set of vias that are connected directly to the cathode of

the diode. The thermal signal also propagates directly toward the sensing diode providing two paths for the heat flux. The spacing between the polysilicon resistor and the aluminum thermal lens, as well as the spacing of the sensing diode from the resistor, determine the response time and the electrical isolation characteristics between the primary and secondary sides of the device. Therefore, the layers used in the structure and the process design rules are intimately coupled with the thermal transducer design process.

The design methodology for a thermal transducer structure is shown in Fig. 2. Typically, the thermal transducer structure is chosen such that the realized isolation voltage will meet or exceed the specified isolation voltage. The fundamental criterion in choosing a transducer structure for a specific application is the above mentioned oxide thickness between the primary and the secondary sides. Due to process layout rules, generally the oxide thickness between the resistor and thermal lens is the determining factor in the achievable isolation of a structure.

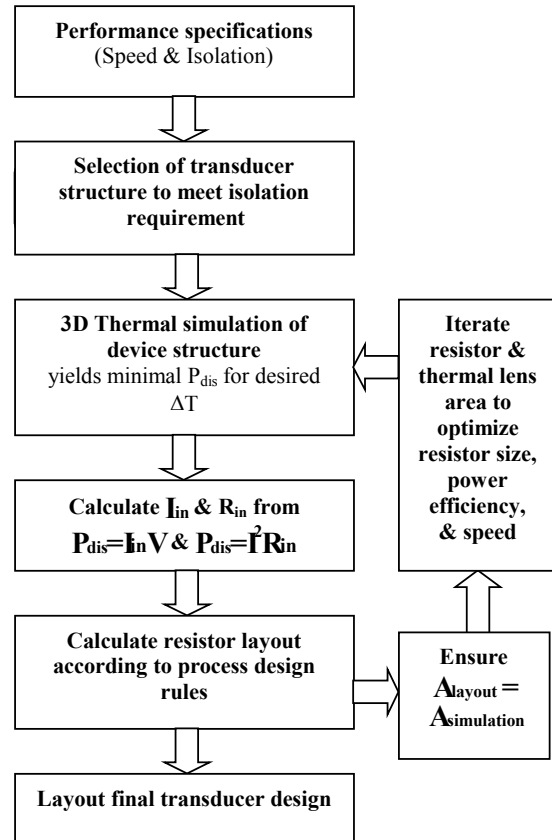


Fig. 2. Thermal transducer design methodology.

In Fig. 1 the oxide layer thickness between the polysilicon and the first level of metal in the process is $\sim 0.5 \mu\text{m}$. The spacing of the diode from the poly resistor is governed by the process layout rules to be about $1 \mu\text{m}$. These distances provide enough information to compute the electrical isolation achievable ($\sim 330 \text{ V}$ maximum for these dimensions) as well as simulate the thermal response time of the device.

Over ten novel structures have been built in the SOI processes listed above [5]. A slightly thicker oxide is achievable using a diffused silicon resistor with an aluminum (Metal 1) lens. The SOI processes used here also have a linear capacitor option that consists of a polysilicon top plate with an n^{++} doped diffused bottom plate. This oxide thickness is about an order of magnitude thinner than the poly to metal 1 oxide, which reduces the amount of required input power and provides faster response times, but at the same time yields a lower electrical isolation rating ($\sim 60\text{V}$).

3. THERMAL TRANSDUCER OPERATION PRINCIPLES

3.1. Thermal transducer primary side

Basically, the primary side of the transducer consists of a resistor. The resistor material (e.g., Si or poly-Si) can vary depending on the transducer structure selected. Once a transducer structure has been chosen according to isolation and speed specifications, a thermal simulator is employed to determine the power dissipated in the resistor that yields a target ΔT ($1\text{--}1.5 \text{ }^\circ\text{C}$) at the diode such that a detectable electrical signal ($\Delta I = 1 \mu\text{A}$) is created. The device was modeled using Flotherm[®] [7], a 3D finite-element thermal simulator. Material properties such as heat capacity and thermal conductivity, among others, were used to accurately model the transient thermal nature of device performance [8, 9].

The power dissipated in the resistor must create enough thermal energy to cause the diode temperature to increase by ΔT in the specified amount of time, e.g., the transducer in Fig. 1 is desired to pass a data bit in less than $1 \mu\text{s}$ to meet I²C bus specifications. The figure of dissipated power, P_{dis} , is found from the 3D thermal simulation, as shown in Fig. 3. Fig. 3 demonstrates the transient thermal analysis of the transducer simulated until steady state is reached, where 25 mW of power (a figure that is found to produce the desired ΔT at the diode) was dissipated in the resistor. The top graph is a plot of the resistor and diode layer temperatures as a function of time for a 25-mW, 500-kHz input signal, and the bottom graph is a snapshot of the top graph demonstrating the thermal response of the resistor and diode. The dissipated power is then used to find the input

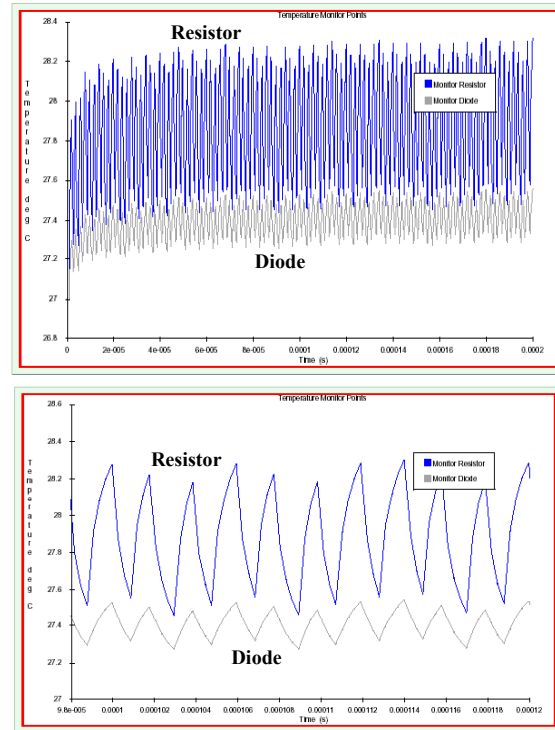


Fig. 3. 3D thermal simulation results demonstrating steady state waveforms of resistor and diode temperatures vs. time (top), and blown up portion of the steady state waveforms of the resistor and diode temperatures vs. time (bottom) for a 25-mW, 500-kHz input.

current, I , needed according to $P_{dis} = IV$, where V is the input voltage. The input current dictates the minimum resistor width that can be realized according to the process current ratings.

The value of the input resistance, R , is also calculated from the dissipated power according to $P_{dis} = V^2/R$. The final layout of the resistor cannot exceed the size constraints of that simulated in 3D, otherwise the effective power density under the thermal lens and thus the change in the sensing diode temperature are reduced (i.e., the simulated structure is too small). If this violation occurs, the 3D simulation process must be repeated to achieve a new power figure, because the original power figure is insufficient for the resistor's resulting thermal mass.

On the other hand, if the original structure analyzed was found to be larger than necessary, then the power dissipation figure is also larger than necessary. Therefore, another iteration with a smaller thermal mass is required to optimize the power efficiency and switching speed of the device. The transducer shown in Fig. 1 was found to

work acceptably well in the range of 20 μm to 40 μm per side.

3.2. Thermal transducer secondary side

The secondary side of the transducer is characterized by a sensing circuit that can transform a change in diode current into a digital signal. The circuit was designed such that a current reference is established against which changing device temperatures are monitored. This sensing circuit dictates the desired diode current for a specific diode voltage. The circuit utilized in testing the transducer in Fig. 1 was found to operate adequately with a diode biased in the range of 2-10 μA for a forward voltage of 0.7 V. Also, the detectable change in current, ΔI , of the diode is 1 μA .

The diode used to detect the thermal signal is sized through device analysis using the Medici[®] finite element simulator package [9]. Given the doping levels and layer thicknesses for the selected process, the diode is implemented in Medici and a sweep of the bias voltage is performed to obtain the current per micrometer. This figure is then used to calculate the diode area that yields the desired current for the bias voltage chosen previously (0.7 V), e.g. the diode used in Fig. 1 yields 129.3 μA at 0.7 V. Utilizing the same diode structure, an electrothermal simulation is then performed to obtain the minimum temperature change, ΔT , that the diode can sense and transition into a detectable ΔI (1 μA).

4. EXPERIMENTAL RESULTS

The test setup shown in Fig. 4a utilizes a MOSFET-based opamp at its core. The non-inverting terminal is connected to a constant V_{ref} of 0.7 V, and the inverting terminal is connected to the anode of the transducer diode, thus forward biasing it at a constant 0.7 V with the diode's cathode tied to ground. A properly sized resistor R_{ref} connects the inverting terminal to the opamp output V_{out} , such that the change in current through the resistor R_{ref} , and ultimately the diode, would yield a measurable change in the output voltage V_{out} .

This test setup yielded unsatisfactory results. The parasitic circuit capacitance and intrinsic device capacitance from the primary side to the secondary side of the transducer dominated the output characteristics of the circuit, thus preventing the detection of the thermal signal.

In order to overcome this problem, a new test circuit was developed that provides a constant forward diode current and measures the change in diode voltage. As shown in Fig. 4b, the circuit utilizes a properly designed current mirror that biases the diode at $\sim 2 \mu\text{A}$, while

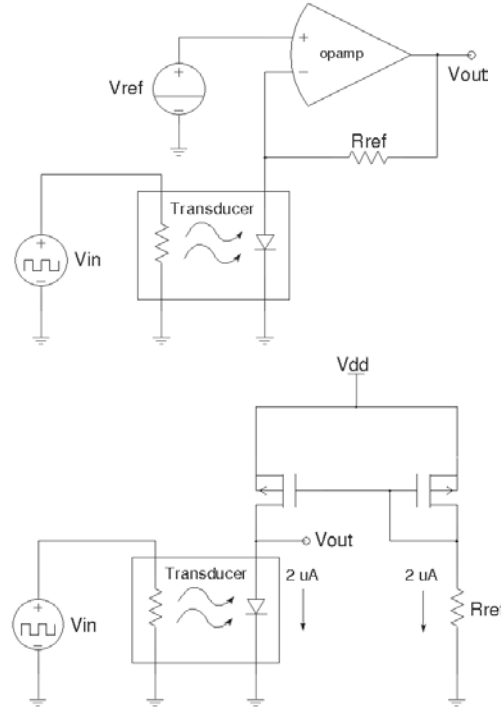


Fig. 4. a) Experimental test setup demonstrating opamp-based test setup (top), and b) current mirror-based test setup (bottom) to verify transducer operation.

measuring the diode anode voltage or output voltage V_{out} .

This test circuit yields valuable information about the response time of the device, even though it does not follow the design procedure outlined above.

The experimental results are shown in Fig. 5a for the device at 1 kHz and in Fig. 5b for its maximum operating frequency of 100 kHz. The experimental results are shown for the “worst-case” duty cycle of 50%, i.e., the spacing between incident data bits is at a minimum for each operating frequency, thus allowing minimal device cooling. In Fig. 5, as the input signal goes high, heat is propagated through the device to the diode. The diode's temperature increases, thus reducing the voltage across it for the constant forward current. The reverse is true when the input signal is low; the diode dissipates heat, thus resulting in an increase in forward diode voltage. In Fig. 5a the thermal response is detected as a decrease in diode anode or output voltage when the input pulse is high, and as an increase in diode anode or output voltage when the input pulse is low. In Fig. 5b the thermal response of the diode can be seen between capacitive spikes.

The intrinsic device capacitance between the primary and secondary side drastically reduces the maximum operational frequency of the device. Consider the output waveform of Fig. 5b. When the input signal rises, a dV/dt

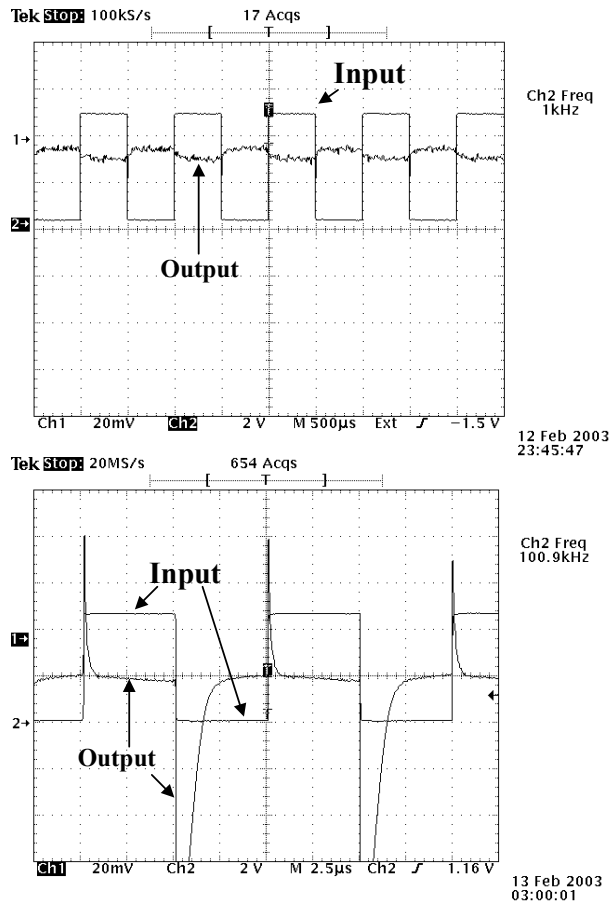


Fig. 5. a) Experimental results at 1 kHz (top) and b) results at 100 kHz for the transducer shown in Fig. 1.

is applied yielding current through the primary-to-secondary capacitance C_{ps} . This excess capacitive current is able to flow through the diode anode, thus producing a small voltage rise in the output. When the input signal falls, a negative dV/dt is applied yielding current from the secondary to the primary side through C_{ps} . The resulting capacitive current must be supplied by discharging of the internal diode capacitance, thus resulting in a large voltage spike across the diode.

This intrinsic device capacitance C_{ps} limits device speed by dominating the output waveforms. As can be seen from Fig. 5, the diode voltage has little time left between the capacitive recovery and the next incident signal. Increasing the frequency of operation will result in the capacitive recovery phase exceeding bit length and the incident signal going undetected.

5. CONCLUSION

Two- and three-dimensional finite element analysis tools were used to analyze a thermal transducer design.

Theoretically, the transducer in Fig. 1 can achieve a propagation delay time on the order of $1\mu s$, which meets I²C bus specifications. Experimentally, the device succumbs to an intrinsic capacitance around 100 kHz. Nevertheless, it is promising that a thermal response can be detected at over 100 kHz, therefore future work will involve elimination of the capacitive effects through device design and external circuit design.

Even though the device is limited intrinsically, it is a novel device that provides *one* solution to *on-chip* isolation issues for low-speed applications. Logic dictates that a thermal-based transducer could suffer from environmental effects created by ambient temperature swings and on-chip localized heating due to circuitry and/or neighboring transducers. Also, of concern could be thermal saturation of the transducer rendering it insensitive to incoming signals. All of these issues are valid concerns. However, each one can be addressed through appropriate external circuitry. Using transducers in dual configurations, where the second transducer is used as a means of isolation between a sensor and control circuitry for shutting down the initial transducer, can address thermal saturation effects. Further, appropriate digital logic on the primary side of the initial transducer propagates signals through the device based on edge detection rather than data values. Likewise, other environmental concerns can be dealt with through additional diode sensors and circuitry and layout rules.

6. ACKNOWLEDGEMENTS

The work described in this paper was performed for the Jet Propulsion Laboratory, California Institute of Technology under contract with the National Aeronautics and Space Administration.

7. REFERENCES

- [1] B.G. Streetman, *Solid State Electronic Devices*, Englewood Cliffs, NJ: Prentice Hall, 1995.
- [2] M. Parameswaran, A. Robinson, D. Blackburn, M. Gaitan, "Micromachined Thermal Radiation Emitter from a Commercial CMOS Process," *IEEE Electron Device Letters*, vol. 12, no. 2, February 1991.
- [3] W. Wojciak, M. Orlikowski, M. Zubert, A. Napieralski, "An Electro-thermal Converter in CMOS Compatible, Front Side Micromachined Technology," *Proceedings of the Mixed Design of Integrated Circuits and Systems Workshop*, Poznan, Poland, June 1997.
- [4] T. McNutt, A. Lostetter, A. Mantooth, M. Mojarradi, "A Novel SOI CMOS Compatible Thermal Device Technology," *Proceedings of THERMES 2002*,

Conference on Thermal Challenges in Next Generation Thermal Systems, Santa Fe, NM, January 2002.

[5] T. McNutt, *Design and Analysis of SOI CMOS-Compatible Thermal Transducers for On-Chip Electrical Isolation*, MSEE Thesis, University of Arkansas, Fayetteville, AR, August 2001.

[6] J.P. Colinge, *Silicon-On-Insulator Technology*, Norwell, MA: Kluwer, 1997.

[7] *Flotherm User's Manual*, Flomerics, Ltd.

[8] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, New York, NY: Springer-Verlag, 1984.

[9] *Medici User's Manual*, Avant! Corp.