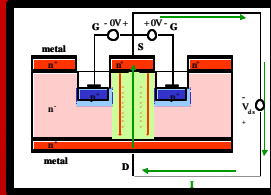


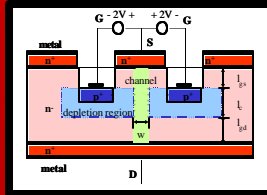


Modeling Vertical Channel Junction Field Effect Devices in Silicon Carbide

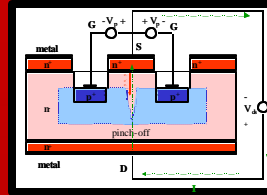


* Electrons are the only mechanism of current flow

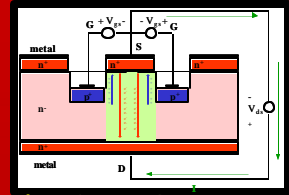
JFET operating in the Unipolar mode



* Notice the reduction in the channel width



* $V_{gs} = V_p$: Pinch - off
* Depletion region not parallel
Channel Pinch-off condition

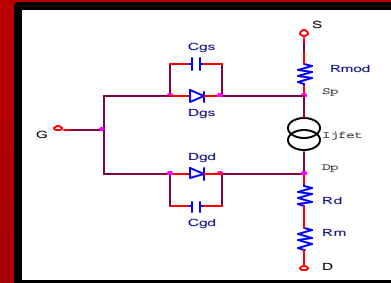


* V_{gs} forward biased
* Electrons and holes conduct

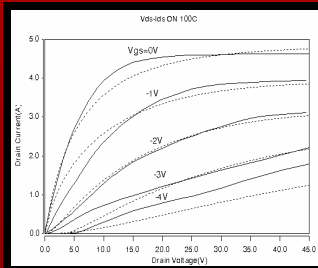
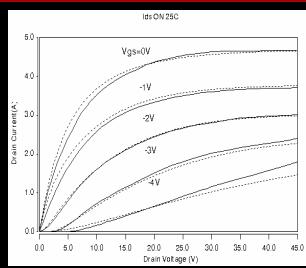
JFET operating in the Bipolar mode

Modeling Methodology

- * Understanding the physics and operation of the device
- * Constructing an internal model topology
- * Developing a set of compact equations for the DC and Transient Characteristics
- * Formulating the model in an HDL - MAST
- * Testing the HDL code in a commercial simulator – Saber
- * Characterizing the device to get data for model validation
- * Validating the model with measured data



Model topology of the SiC JFET



Measured (solid) and simulated (dashed) On-state waveforms of the SiC JFET at 25°C (left) and 100°C (right)

Characteristic Equations

JFET/SIT channel currents

$$I_p + I_n = I$$

$$\text{if } V_{ds} > 0$$

$$I_{ge} = i_p [1 + \tanh(P_d(V_{gs} - V_p))] \cdot \tanh(aV_{ds}) \cdot e^{-\gamma V_{ds}}$$

$$P_d = 1 + 0.05(V_{gs})$$

Transient Equations

$$W_{gs} = \sqrt{\frac{2\epsilon_{sc}(V_{gs} + V_{gs0})}{qN_D}}$$

$$C_{gs} = \frac{L_{gs} A_{gs} \epsilon_{sc}}{W_{gs}}$$

$$W_{gd} = \sqrt{\frac{2\epsilon_{sc}(V_{gd} + V_{gd0})}{qN_D}}$$

$$C_{gd} = \frac{A_g \epsilon_{sc}}{W_{gd}}$$

On-State Equations

$$W = W_{bc} - W_{gd}$$

$$R_{sd} = \frac{W}{qN_D m_e (A_g + A_s)}$$

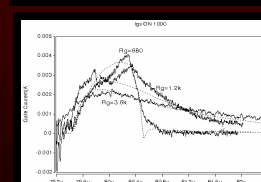
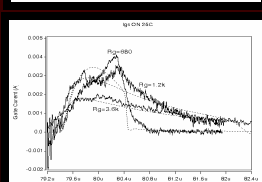
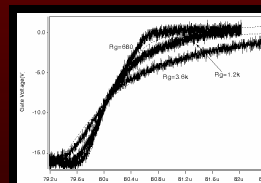
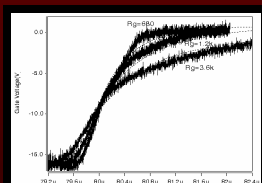
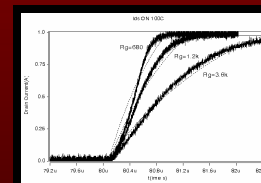
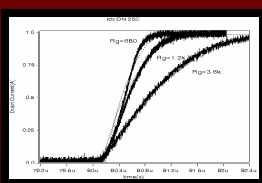
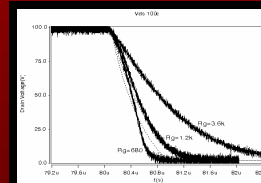
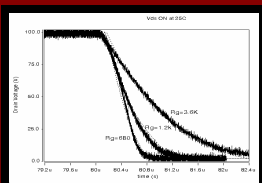
$$m_e = \frac{947}{1 + \frac{N_D}{1.94 \times 10^{17}}} - 215$$

$$q_{in} = I_{gs}$$

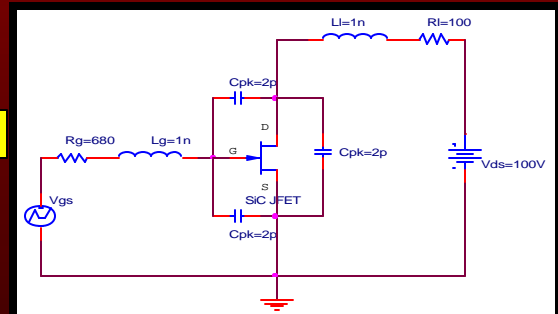
$$i_{sd} = \frac{(m_e + m_h) V_{gs} q_{in}}{W_{sd}^2}$$

$$I_{gd} = I_{gs} \exp(V_{gs}/m_g V_T) - I$$

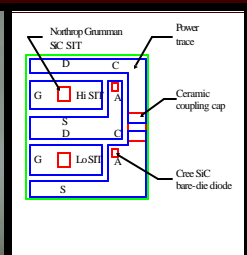
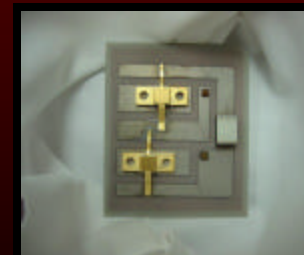
$$I_{gs} = I_{gs0} \exp(V_{gs}/m_g V_T) - I$$



Measured (solid) and simulated (dashed) turn-on waveforms of the SiC JFET at 25°C (left) and 100°C (right) (a) drain voltage (b) drain current (c) gate voltage (d) gate current



Simulation test bench for the transient analysis of the SiC JFET



SiC SIT Half Bridge (500W) designed by the Arkansas SiC Group